The Future of FPGA Forth

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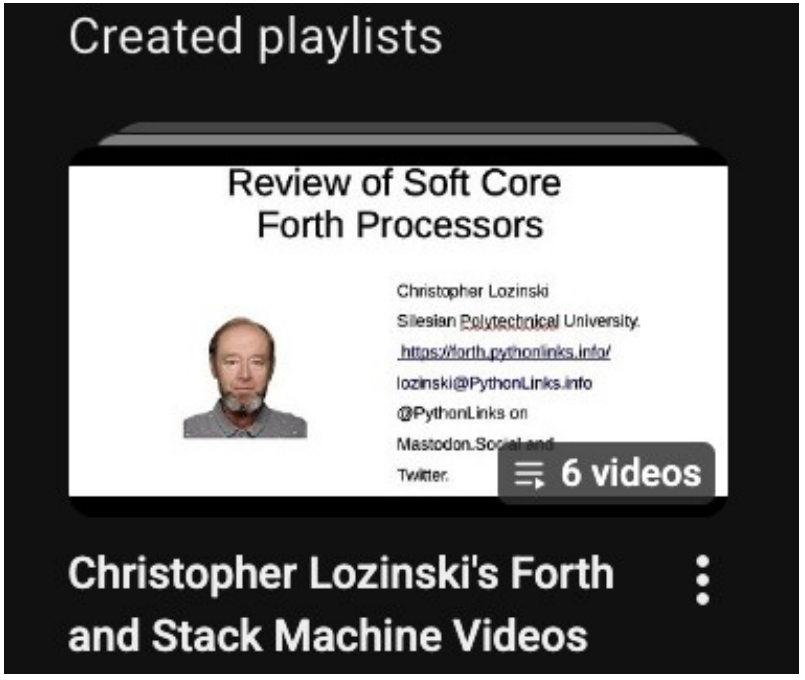
Forth Discord Server

Pico-Ice Discord Server

Hana-1 Discord Channel

Past Talks



Six Forth Videos
on my
Youtube Playlist

Hana 1, ½ the RISC-V Size

	1162 LUTs	SwapForth J1a
-	140 LUTs	Remove the Memory Multiplexer
-	512 LUTs	Use BRAMs for two 256 deep 16 bit stacks
	500 LUTs	The size of the Bit Serial RISC-V Serve CPU.
	1150 LUTs	Typical small RISC-V size.

Stack Machines have Smaller Memory

WASM Design Rationale

“The stack machine allows smaller binary encoding than registers or Static Single Assignment Form.”

Stack Vs Register Machine Memory

Stack Machines

6-8 Bits for a Stack Machine Instruction. Eg: MicroCore UXN

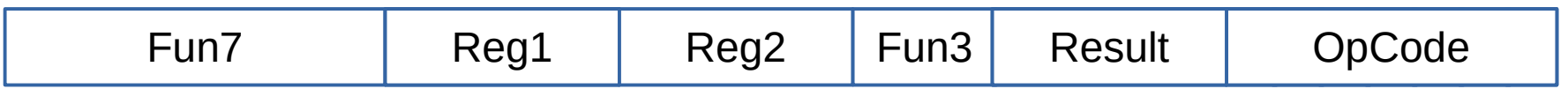
L = Literal

3 OpCodes in 16 bits. Eg EP16, b16

5 opCodes in 32 bits. Eg EP32

RISC-V

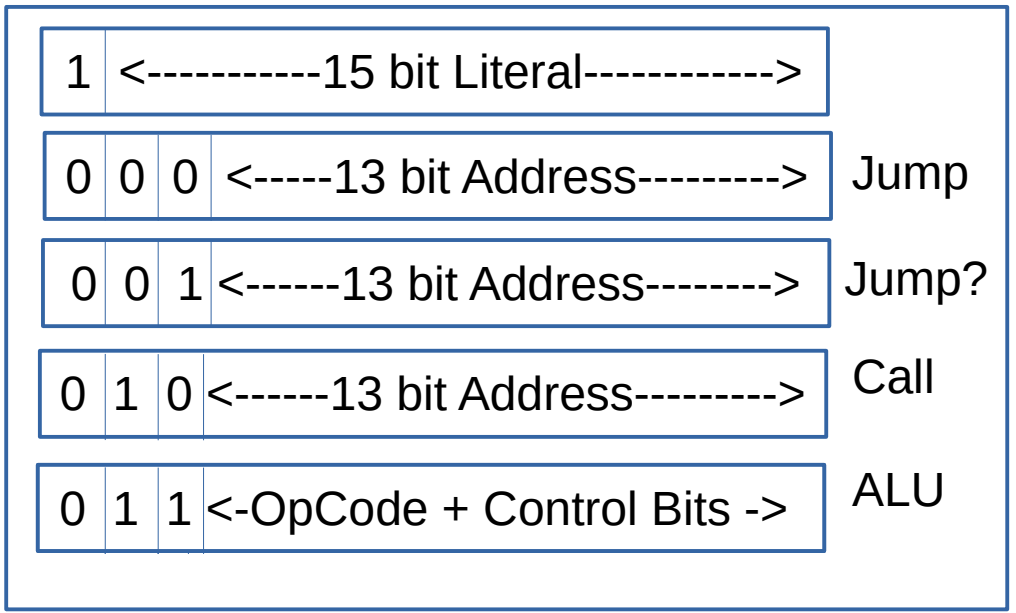
3 * 5 bits for two operands and a results register and 7->17 bits OpCode = 22->32 bits Risc-V



Second Generation Stack Computer Architecture

J1 Vs RISC-V Memory

J1



RISC-V

3 * 5 bits for two operands and a results register and 7->17 bits OpCode = 22->32 bits

Fun7	Reg1	Reg2	Fun3	Result	OpCode

[Second Generation Stack Computer Architecture]

Frequency Problem

- Hana 1 (22 Mhz)
- RP2350 (2 x 150 Mhz)
- Large RAM SPRAM (75 Mhz)
- Block RAM (PSRAM) (150 Mhz)

4 Stage RISC-V Pipeline

https://studyelectrical.com/2023/09/fpga-gpu-cpu-asic-differences.html

No Registers Problem

RISC-V has 32 Registers

register	ABI	description
x0	zero	Hardwired zero
x1	ra	Return address
x2	sp	Stack pointer
x3	gp	Global pointer
x4	tp	Thread pointer
x5	t0	Temporary 0
x6	t1	Temporary 1
x7	t2	Temporary 2
x8	s0/fp	Saved register0/frame pointer
x9	s1	Saved register 1
x10	a0	Function argument/return value 0
x11	a1	Function argument/return value 1
x12	a2	Function argument 2
x13	a3	Function argument 3
X14	a4	Function argument 4
x15	a5	Function argument 5

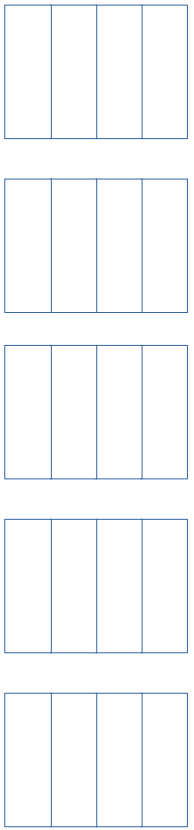
register	ABI	description
x16	a6	Function argument 6
x17	a7	Function argument 7
x18	s2	Saved register 2
x19	s3	Saved register 3
x20	s4	Saved register 4
x21	s5	Saved register 5
x22	s6	Saved register 6
x23	s7	Saved register 7
x24	s8	Saved register 8
x25	s9	Saved register 9
x26	s10	Saved register 10
x27	s11	Saved register 11
x28	t3	Temporary 3
x29	t4	Temporary 4
x30	t5	Temporary 5
x31	t6	Temporary 6
pc	-	Program counter

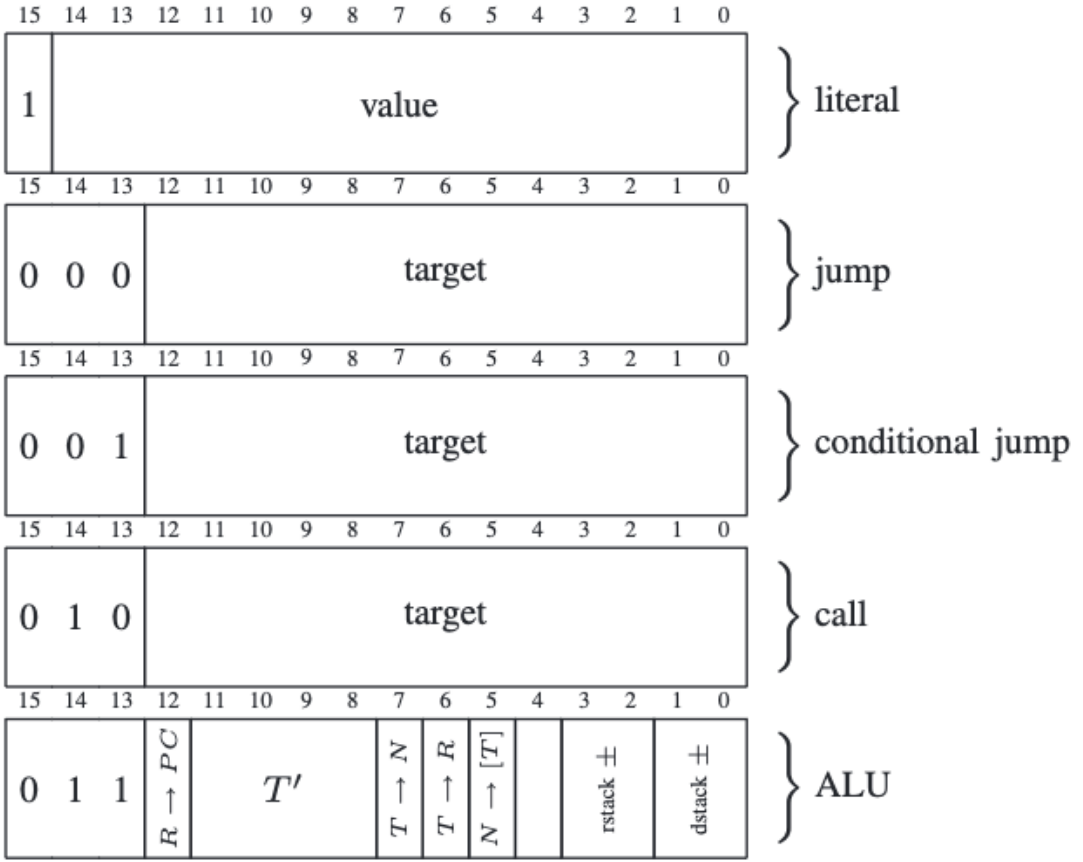
Instruction Format

4 Extra bits give each subroutine 8 registers for read and write above stack.

GateMate has 20 bit wide 1024 word deep memories.

Lattice NX 17/33/40 have 18 wide by 1024 word deep memories.





Interpreter Requires Memory Problem

- J1 requires 8K words of memory
- What if we want 20 J1s?

CustomAsm

```
#ruledef
{
    load r1, {value: i8} => 0x11 @ value
    load r2, {value: i8} => 0x12 @ value
    load r3, {value: i8} => 0x13 @ value
    add  r1, r2          => 0x21
    sub  r3, {value: i8} => 0x33 @ value
    jnz  {address: u16}  => 0x40 @
address
    ret                  => 0x50
}
```

```
multiply3x4:
    load r1, 0
    load r2, 3
    load r3, 4

    .loop:
        add r1, r2
        sub r3, 1
        jnz .loop

    ret
```

Farewell To Forth

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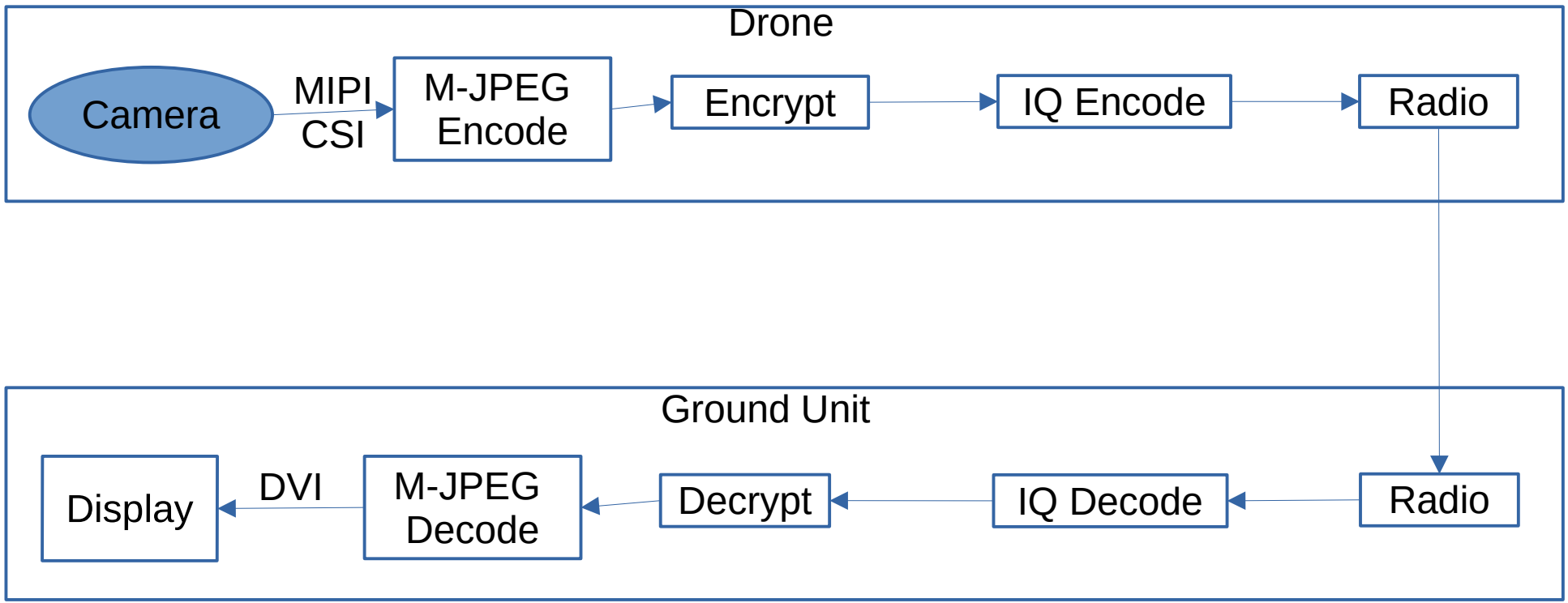
Drone Video Pipeline



Wiki.PythonLinks.info

Video Processing Wiki

Open Source Video Processing Wiki

Open Source Video Processing Wiki

This is a wiki about processing video in real time using microcontrollers, ASICs and FPGAs.

Questions?

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