



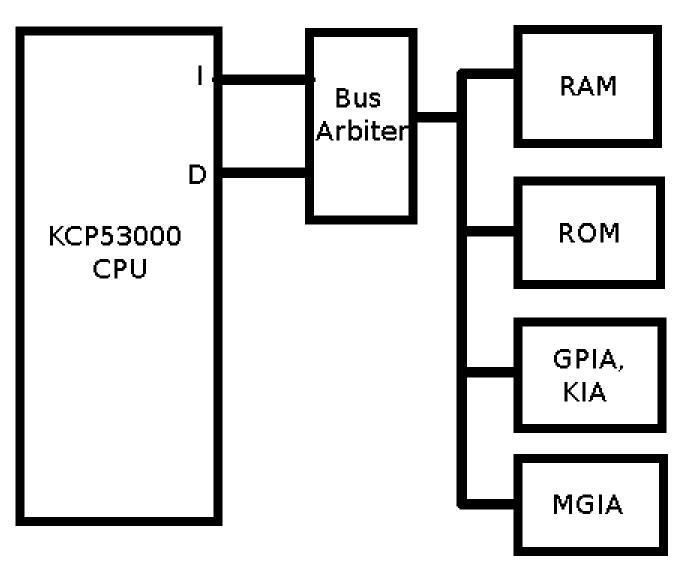
Kestrel Computer Project

Kestrel-3

Running eForth 1.0!

- \* Obviously, software emulation works. ;-)
- \* KCP53000 CPU design in Verilog now available via GitHub. https://github.com/kestrelcomputer/polaris
- \* Physical CPU != Emulated CPU
  - \* CSRs are different
  - \* Performance is different
  - \* Physical CPU supports interrupts.
- \* eForth 1.0 ported to run in firmware!
  - \* It's powering this slide show right now.
  - \* BLOCKs only for now. No filesystem.

Crude Block Diagram



- \* Except for video refresh, no specialized hardware acceleration.
- \* Runs more or less around 6 MIPS in emulation.
- \* Expected to run about the same in physical hardware.

#### But, there's a problem:

- \* eForth's compiler runs much more slowly than anticipated.
- \* Around 1 second to compile 1024 bytes of Forth code.
- \* Perfect opportunity for anyone interested to contribute!

If you're interested in helping the Kestrel Project, and are willing to learn my RISC-V development tools (they are proprietary, but not hard to learn), this is a great opportunity to contribute to the project.

You can reach me via e-mail at <kc5tja@arrl.net>. Or, visit the project page on Github:

https://github.com/kestrelcomputer/kestrel

# Thank you for your attention!

Q & A