Debug an FPGA with a Tiny Interpreter

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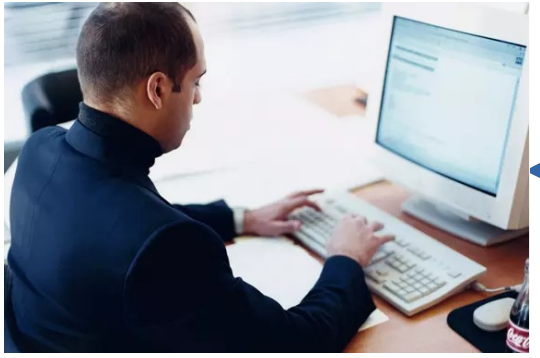
Python TestBench + Simulator

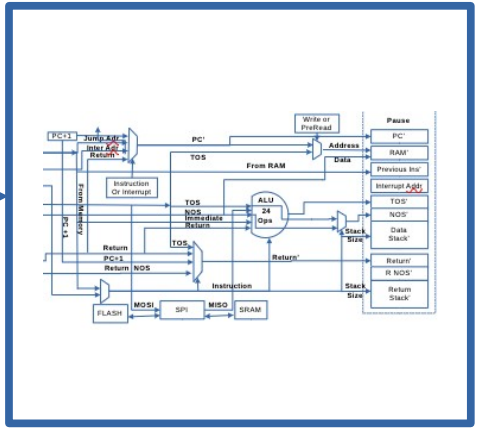
cocotb

Python Interpreter

Simulator



Interprocess Communication

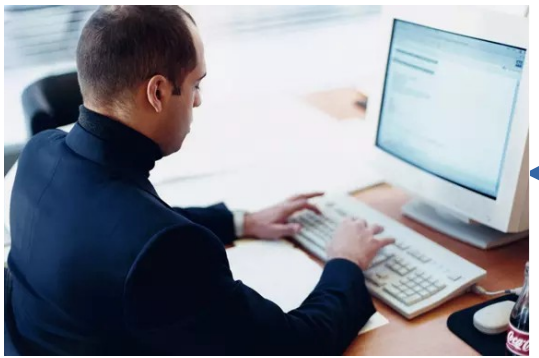


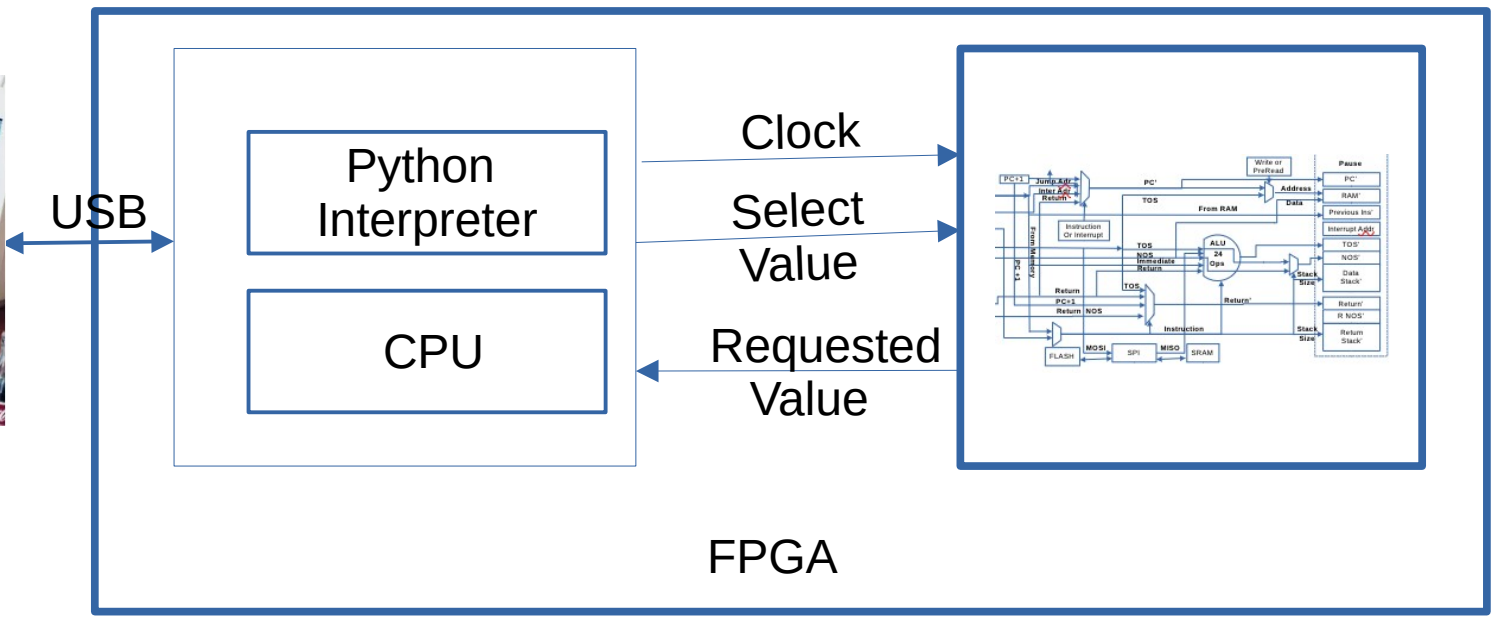
Python on the FPGA

Desktop PC

Soft Core + Interpreter

Design Under Test/Debug





Python Memory Requirements

MicroPythons minimum requiremenst are 256KByte of ROM and 16KB RAM.
Snek requires 32KBytes ROM + > 1KByte RAM
The Lua interpreter takes 282KBytes and the Lua library takes 470KBytes.
eLua requires 5.4 KBytes of RAM.

ROM is slower than RAM

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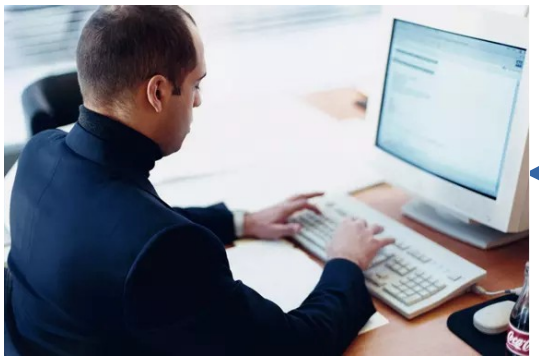

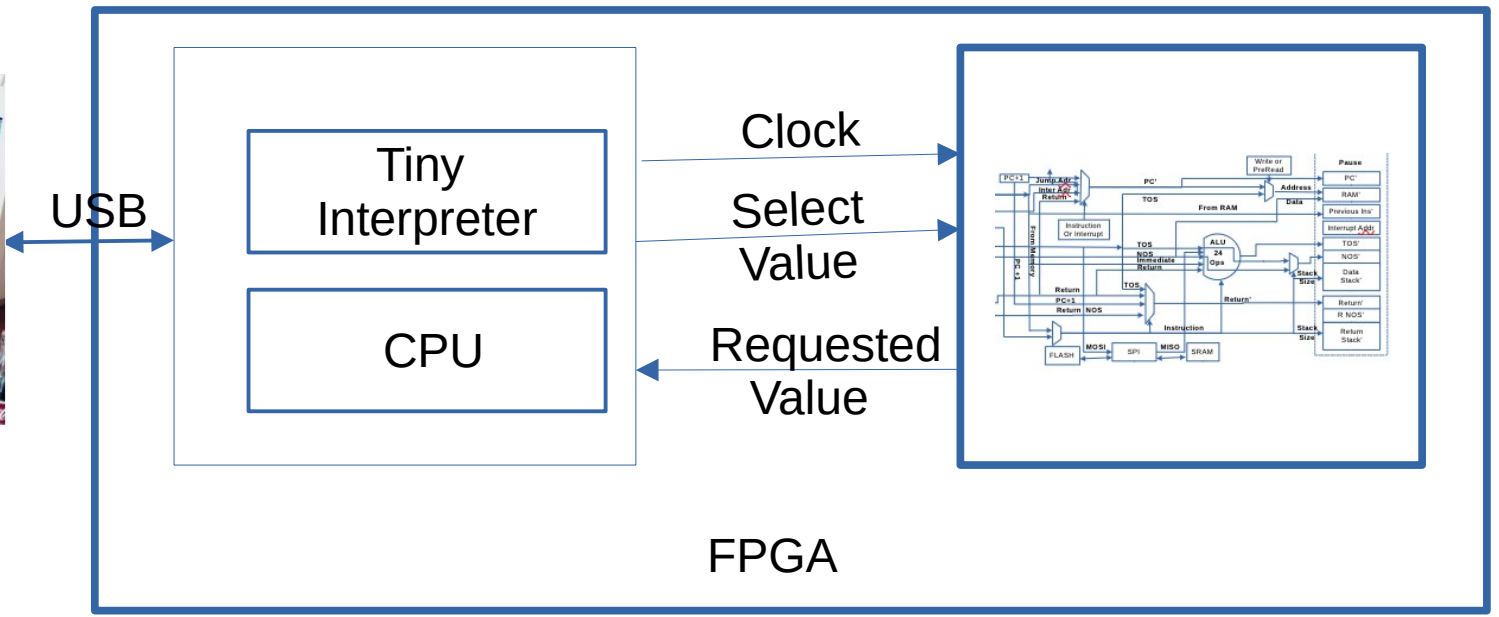

Tiny Interpreter on the Simulator

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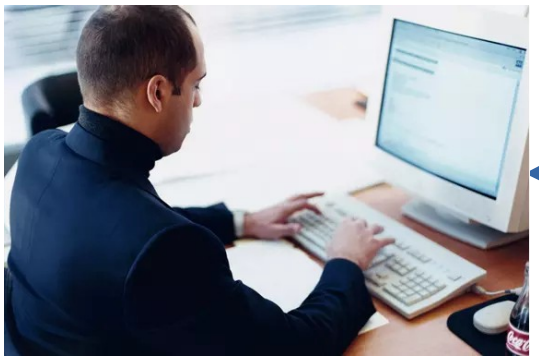
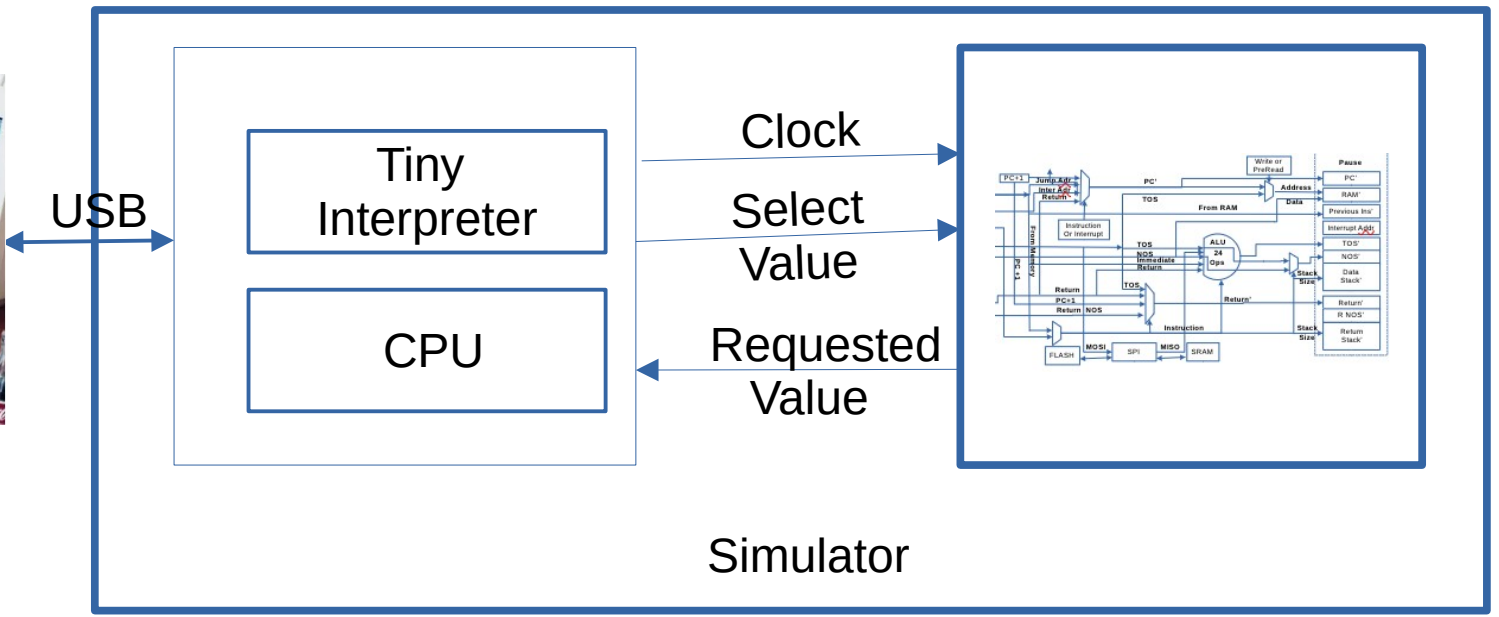




Lattice Documentation

5. SPRAM Content during Warmboot

During configuration through Warmboot, SPRAM content is not loaded. Thus, previous data on the SPRAM are retained.

Below is a standard configuration procedure:

1. At the beginning of the configuration, all the SRAM has been cleared to *0*,

POWEROFF	This pin turns off the power to the memory core. Note that there is no memory data retention when this is driven low.

What is this Tiny Interpreter?

Mecrisp Ice Forth requires > 1.5 KBytes RAM. No ROM.
Runs on both the Simulator and on the FPGA

Python

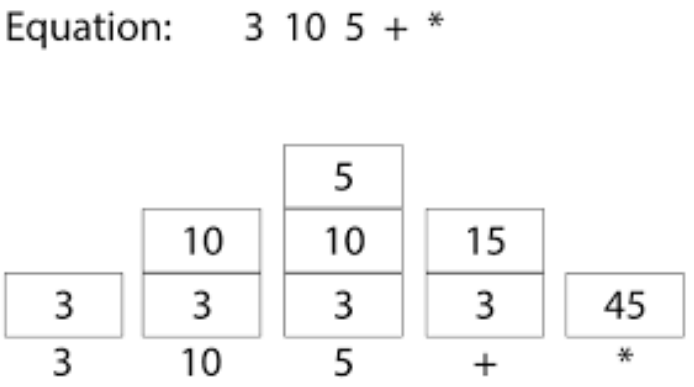
print((10 + 5) * 3)

>>> 45

Forth

3 10 5 + * print

>>> 45



Questions

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