GateMate is For Forth

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SVFIG

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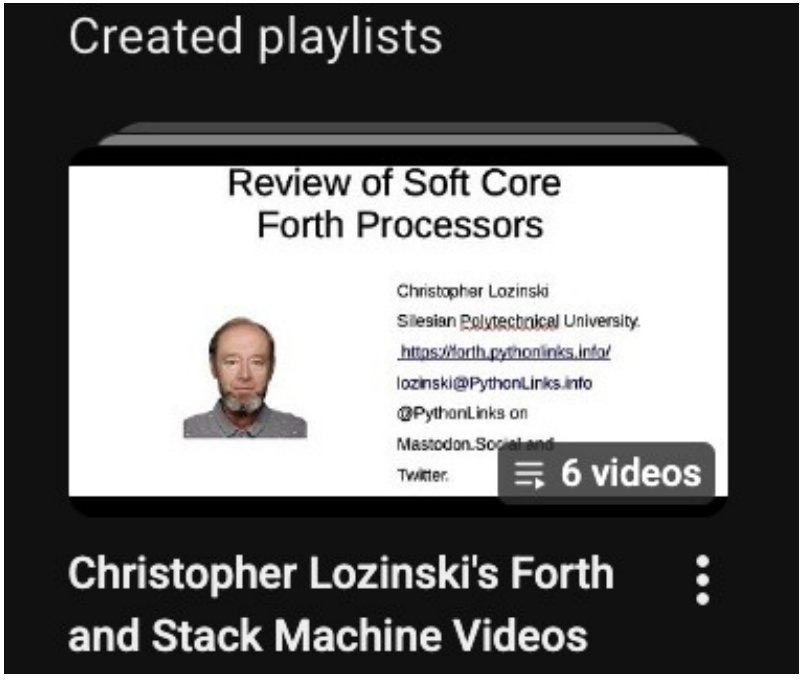
Ulx5M Discord

Olimex Discord

Past Talks

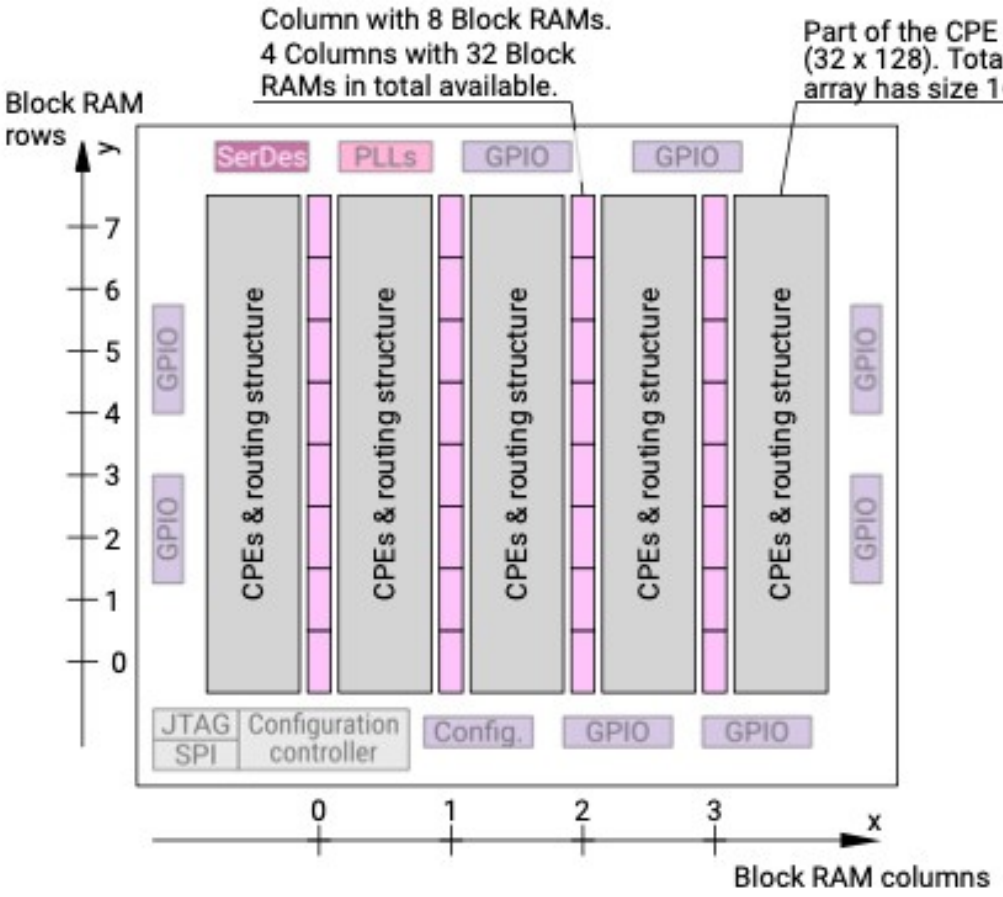


Seven Forth Videos
on my
Youtube Playlist

Hana 1, ½ the RISC-V Size

	1162 LUTs	SwapForth J1a
-	140 LUTs	Remove the Memory Multiplexer
-	512 LUTs	Use BRAMs for two 256 deep 16 bit stacks
	500 LUTs	The size of the Bit Serial RISC-V Serve CPU.
	1150 LUTs	Typical small RISC-V size.

Block RAM



1_310_720 bits

1,2,5,10,20,or 40 wide

Too many options to describe

Instruction Format

4 Extra bits give each subroutine 8 registers for read and write above stack.

GateMate has 20 bit wide 1024 word deep memories.

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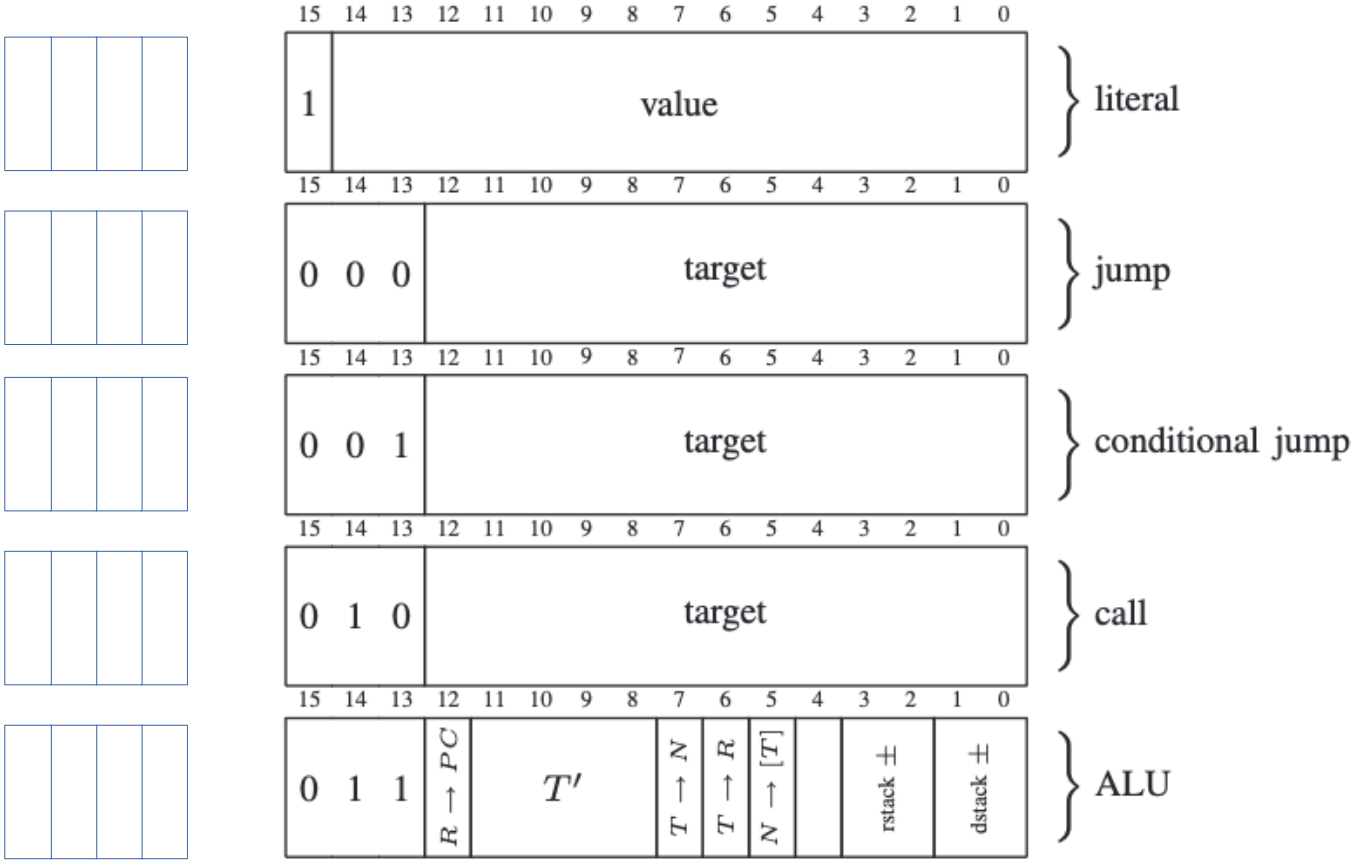
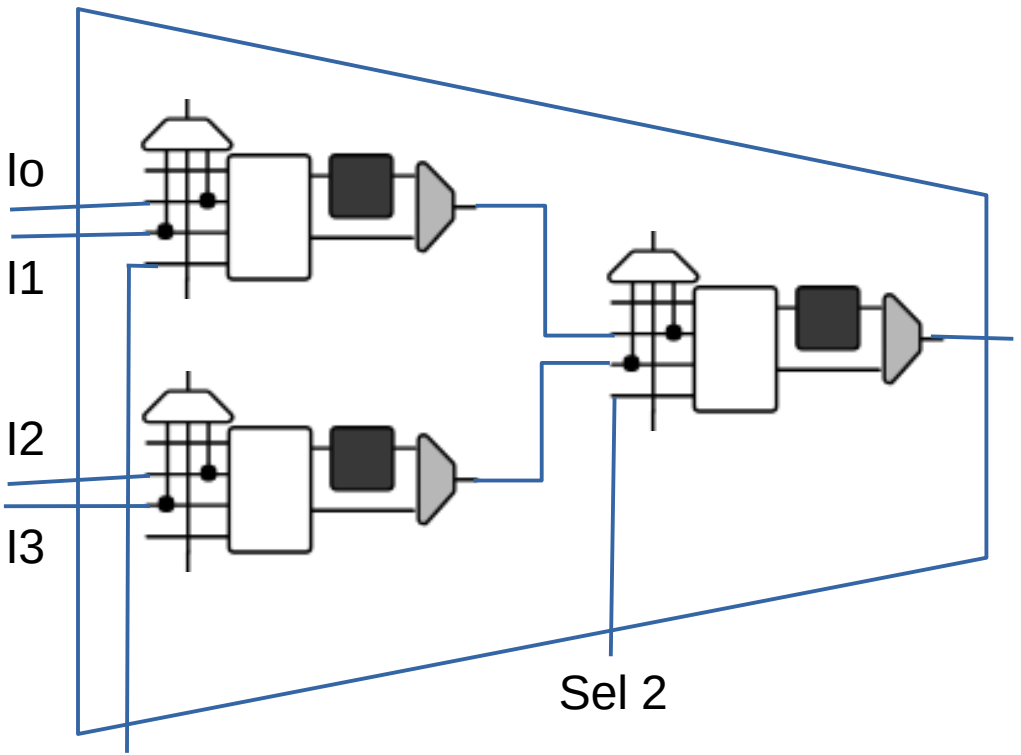
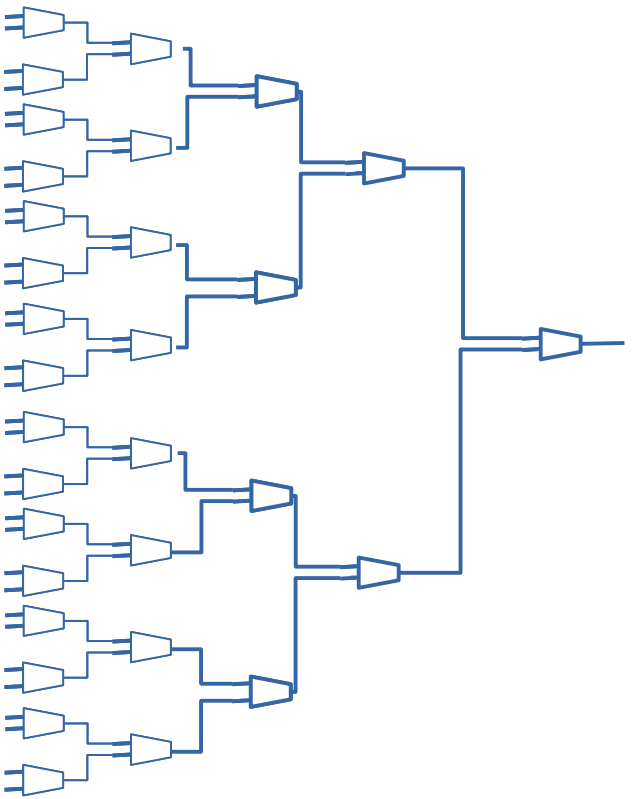


Multiplexing

2 inputs * 32 registers * 31 LUTs/bit = 1984





CustomAsm

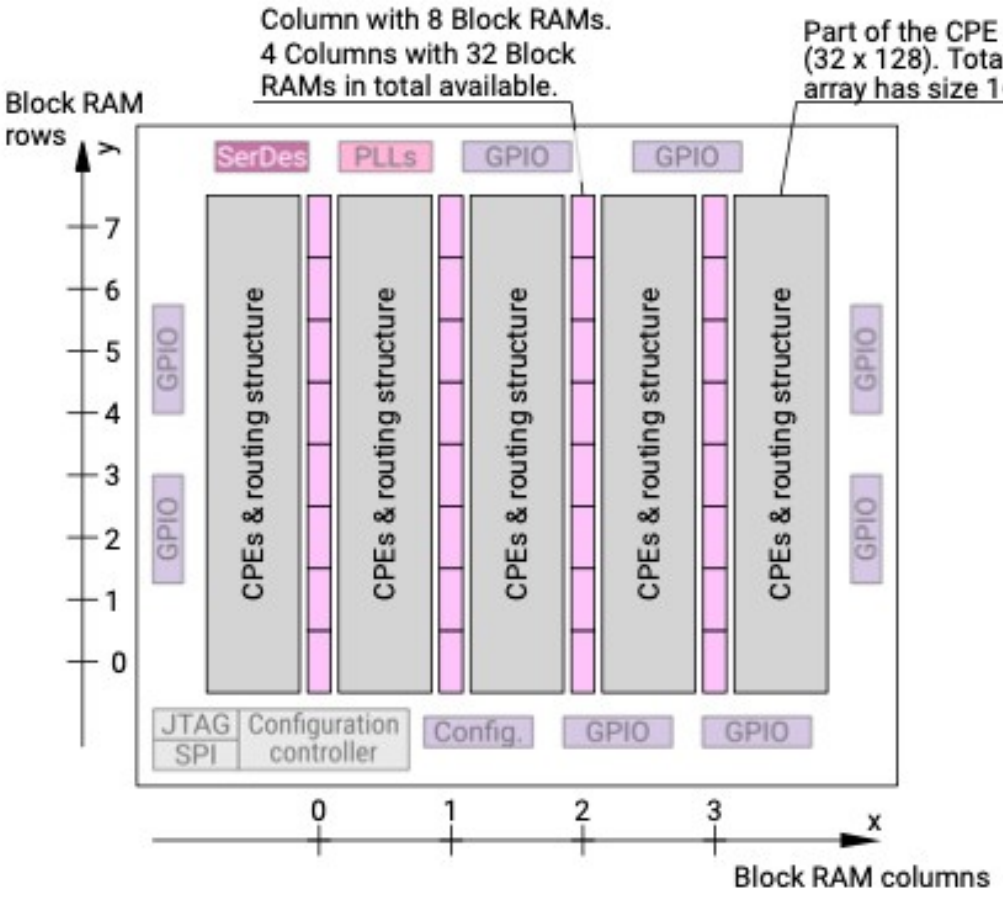
```
#ruledef
{
    load r1, {value: i8} => 0x11 @ value
    load r2, {value: i8} => 0x12 @ value
    load r3, {value: i8} => 0x13 @ value
    add  r1, r2          => 0x21
    sub  r3, {value: i8} => 0x33 @ value
    jnz  {address: u16}  => 0x40 @
address
    ret                  => 0x50
}
```

```
multiply3x4:
    load r1, 0
    load r2, 3
    load r3, 4

    .loop:
        add r1, r2
        sub r3, 1
        jnz .loop

    ret
```

Block RAM



1_310_720 bits

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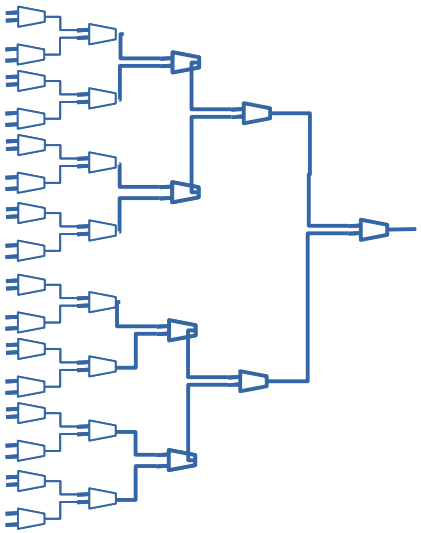
Low end FPGAs

	Gowin	ICE40	GateMate	ECP5	NX17
Price	NA	$8	$15	$15	$25
Bit Width		16	20	18	36
LUTs		5K	20K	12K	17K
Large RAM		4 SP RAMs 2**16 words	64 DP RAMS 1024 Words		5 DPRams 2**16 words
Small Width		16		18	18
Small Rams		30		32	24
Multipliers			< 142 18*18	18 18x18	24 18x18
Forth Cores		4	6	3	5
Stack Cores		8	16	8	6

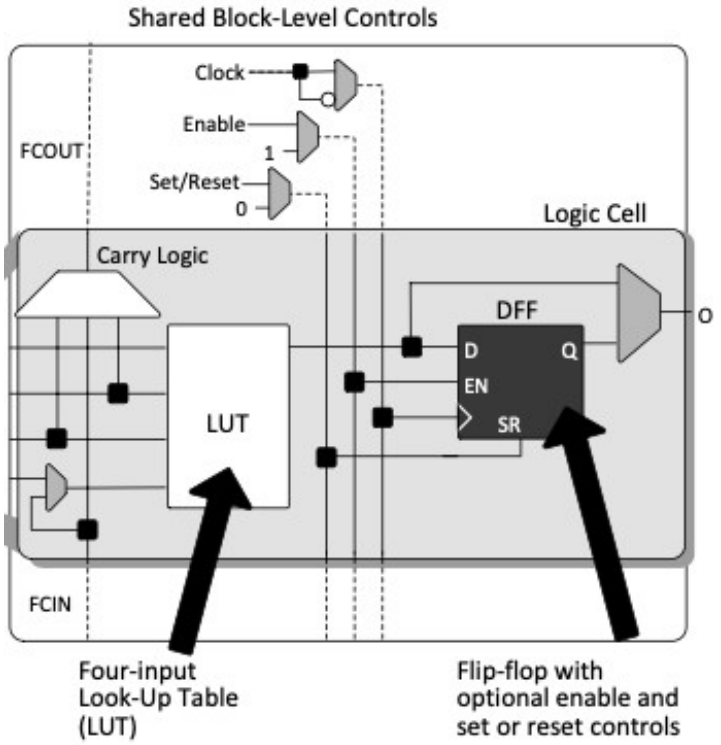
Frequency Problem

- Hana 1 (22 Mhz)
- RP2350 (2 x 150 Mhz)
- Large RAM SPRAM (75 Mhz)
- Block RAM (PSRAM) (150 Mhz)

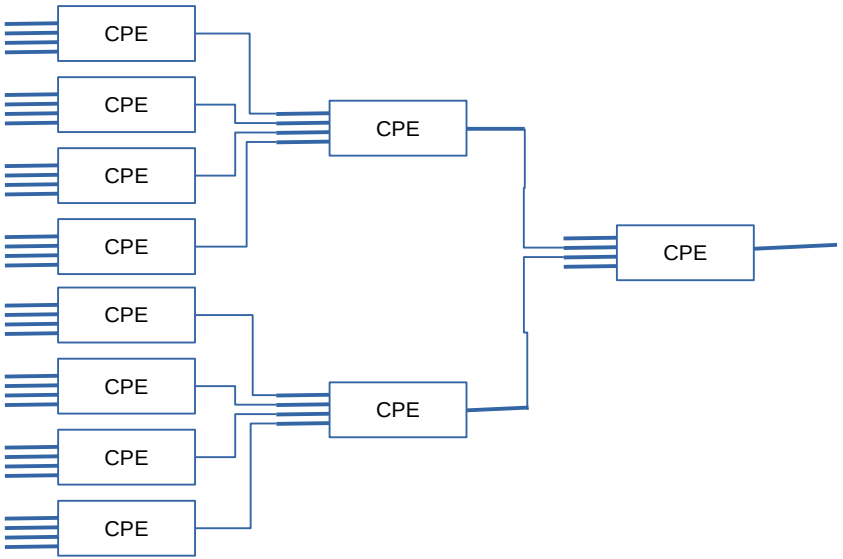
32 Bit Multiplexer

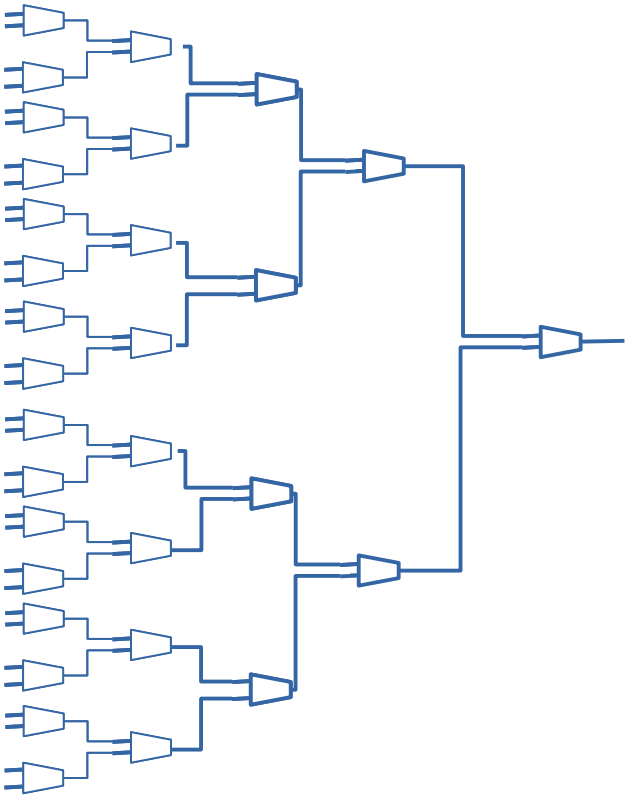


A 32 Bit Multiplexer requires 31 Lattice 4-input LUTs. RISC-V requires 32 Registers, each with 31 4LUTs, or 996 LUTs. 1988 for two arguments.

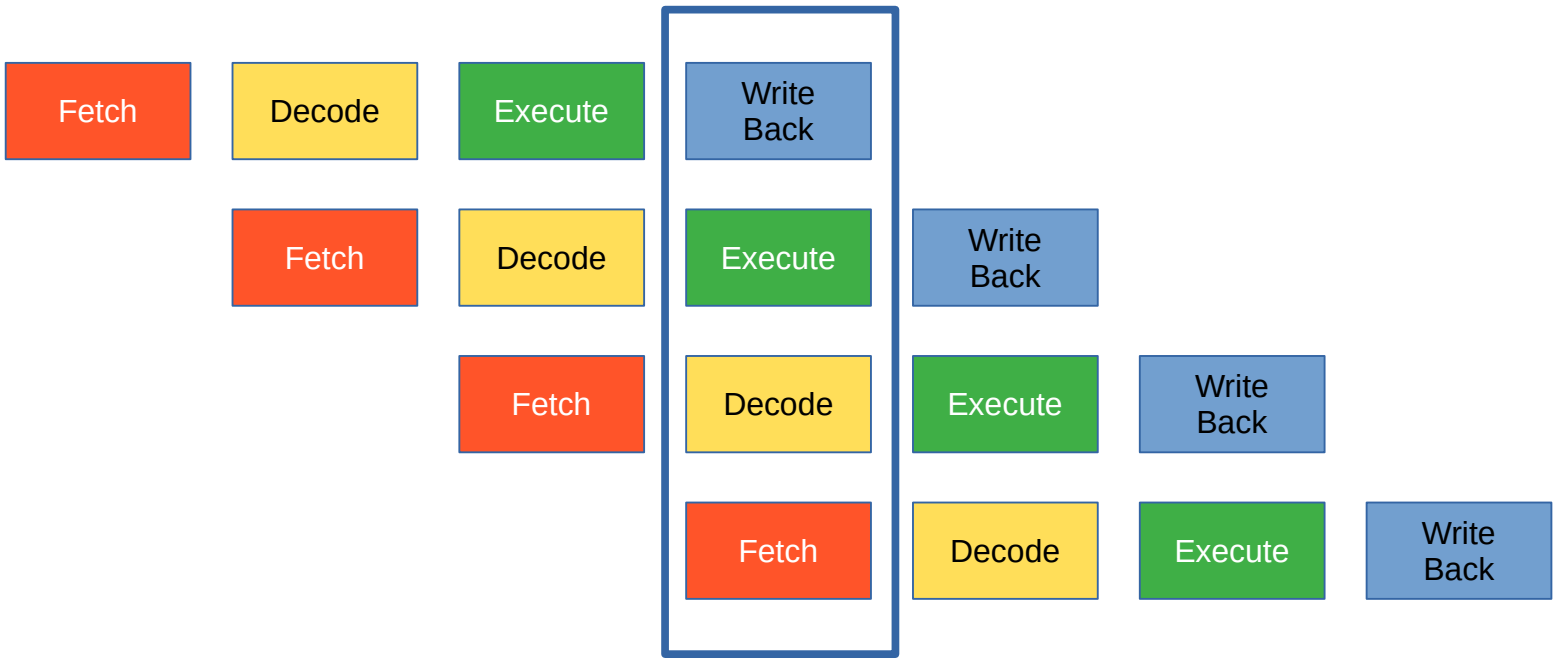


GateMate Vs Lattice Multiplexer

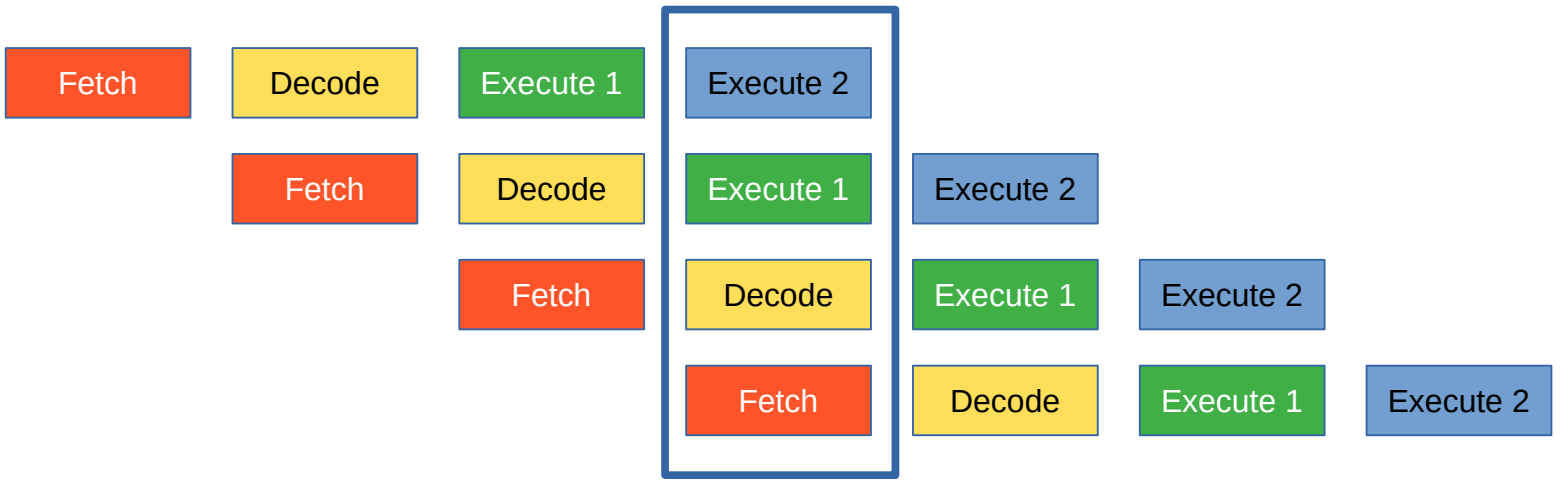




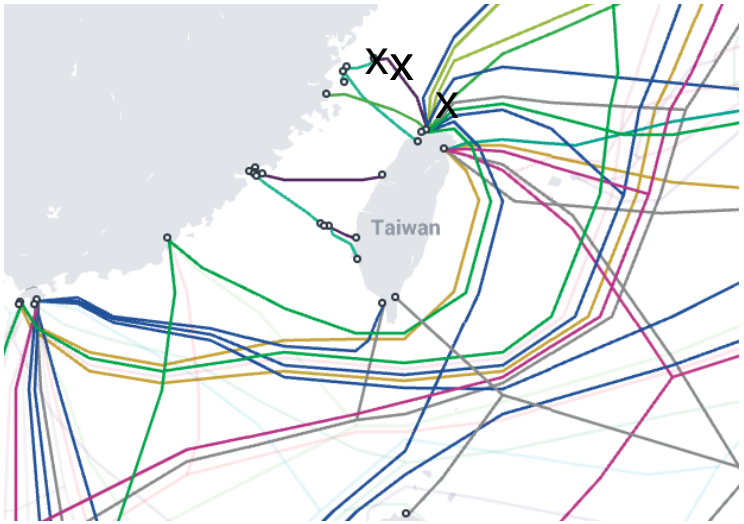
RISC-V Barrel Processor



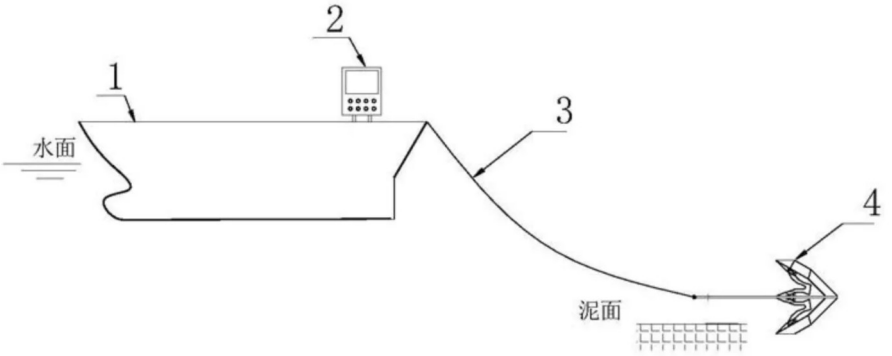
Stack Machine Barrel Processor



TSMC Risks



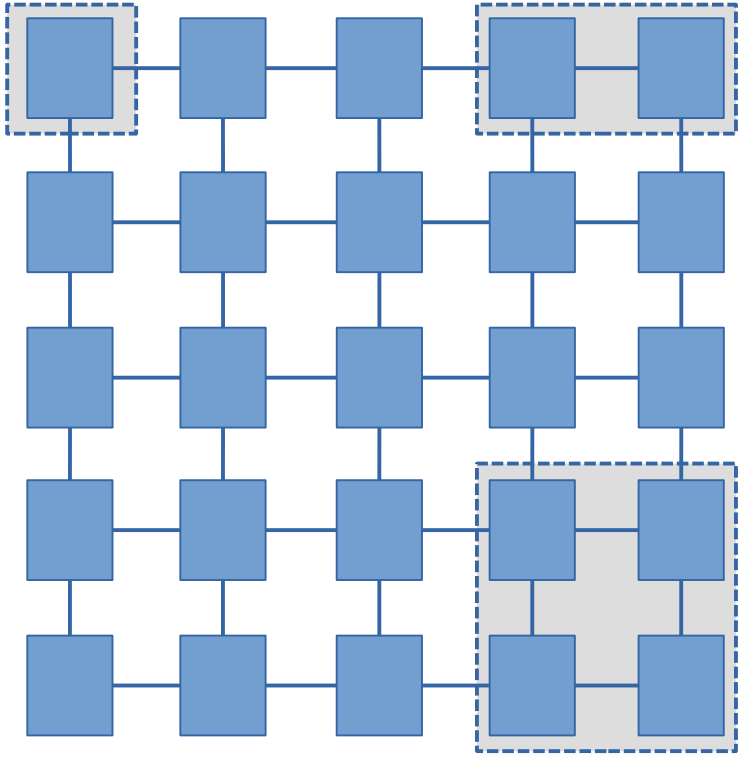
Locations of Cable Cuts



Chinese Patent on Cutting Cables

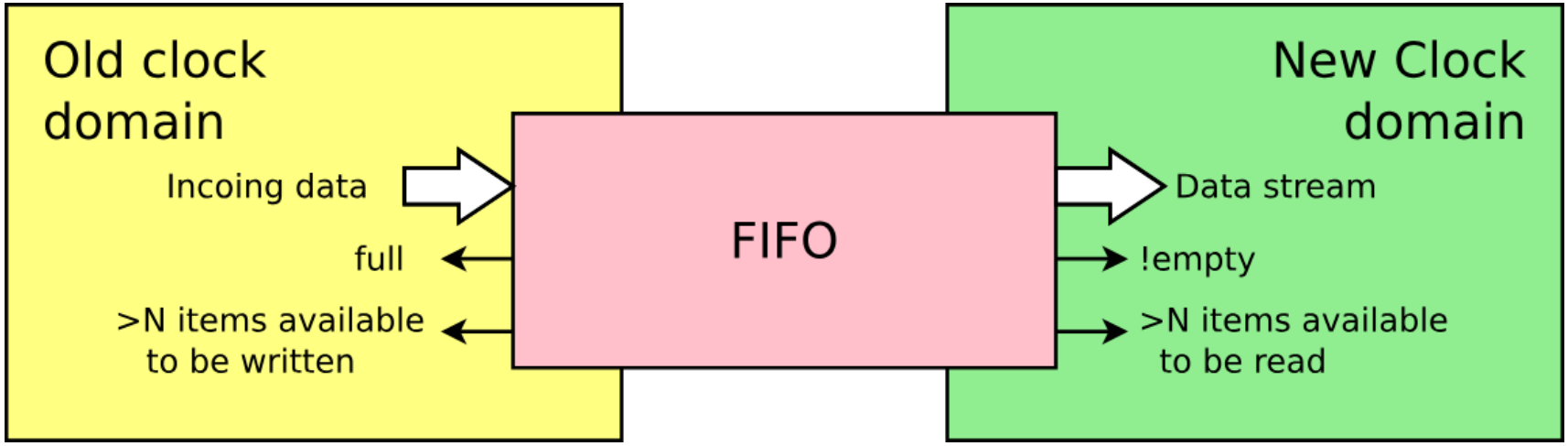
“Taiwan is a sacred and inseparable part of China's territory.” - China

Many Cores From 1 Mask Set



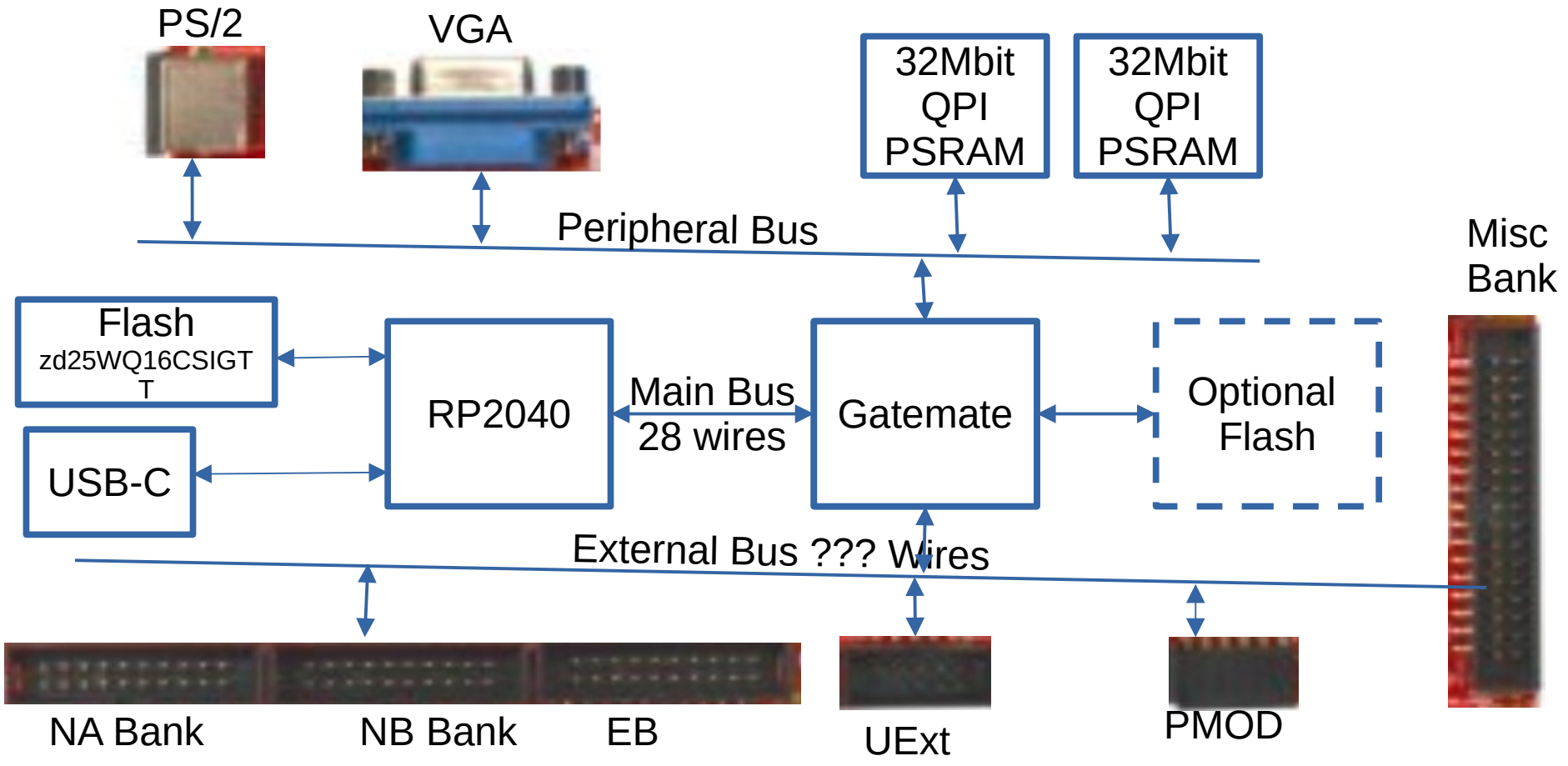
Wafers are sliced into die and packaged. Currently each die can have 1, or 2 GateMate cores. With new packaging it is possible to have up to 25 cores in a single die. 500,000 CPEs, 32Mbits and 25 Serdes.

Clock Domain Crossings

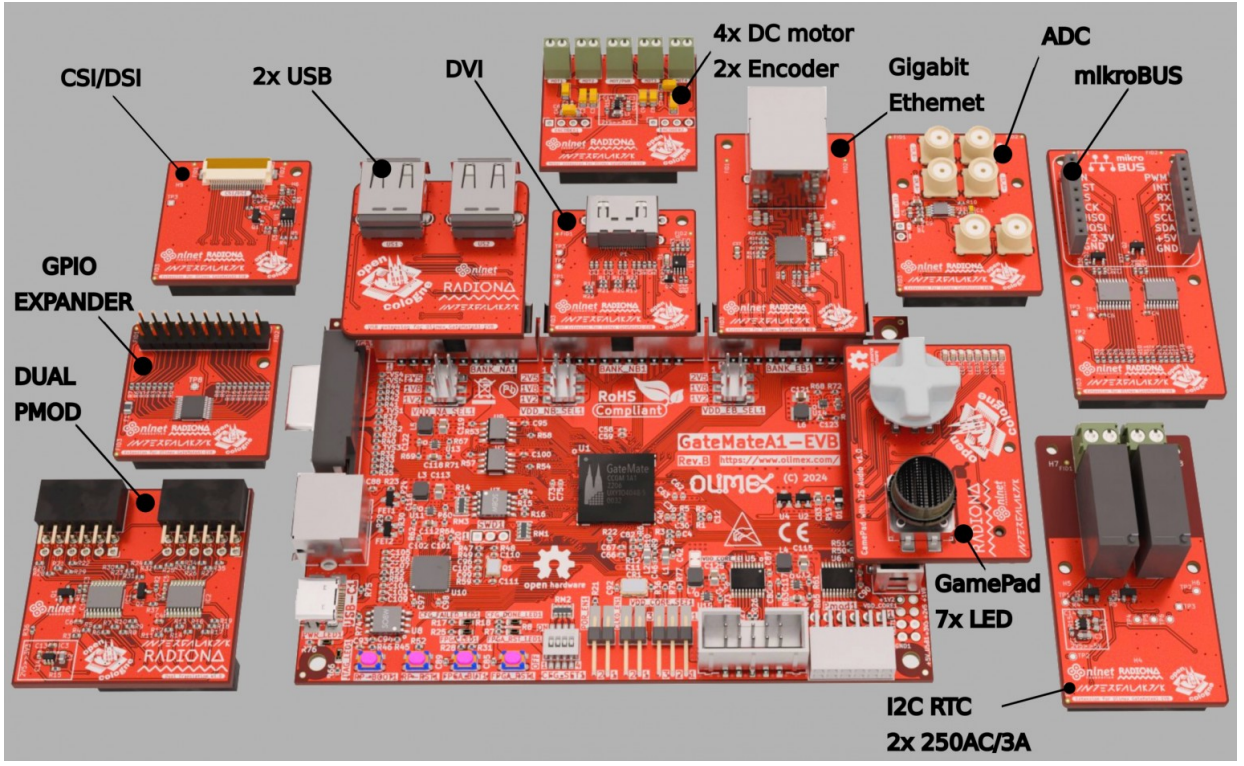


GateMate includes FIFO queues for Clock domain Crossings.

50 € Olimex GateMate Board



GateMate AddOns



ADC

I2S Audio

MicroBusIO

2 USB Host Ports

Camera Port

DVI
Ethernet
Power
Timer
Simple I/O

System On a Board

	Pico Ice	Olimex GateMate	Ice V wireless
MCU	RP2040	RP2040	ESP32-C3-MINI-1
RP ← -> Wires	12	28	?
# of BRAMS	30	64	30
BRAM Elements	256	1024	256
BRAM Width	16 bits	20 bits	16 bits
Large Ram	4*2**16 bits	0	4*2**16 bits
# Logic Elements	5280	20,000	5280
DSPs	8 16x16	<400 8*8	8 16x16
Case	None	12 Euro	None
Price	$38 + VAT	$50 + 0	$99.00 USD

Questions

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July 2025

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