RESTORING AN APOLLO GUIDANCE COMPUTER

Block II prototype #14 used to ‘man-rate’ the lunar module in the thermal/vacuum test chamber at MSC Houston - scrapped!

AGC Block II

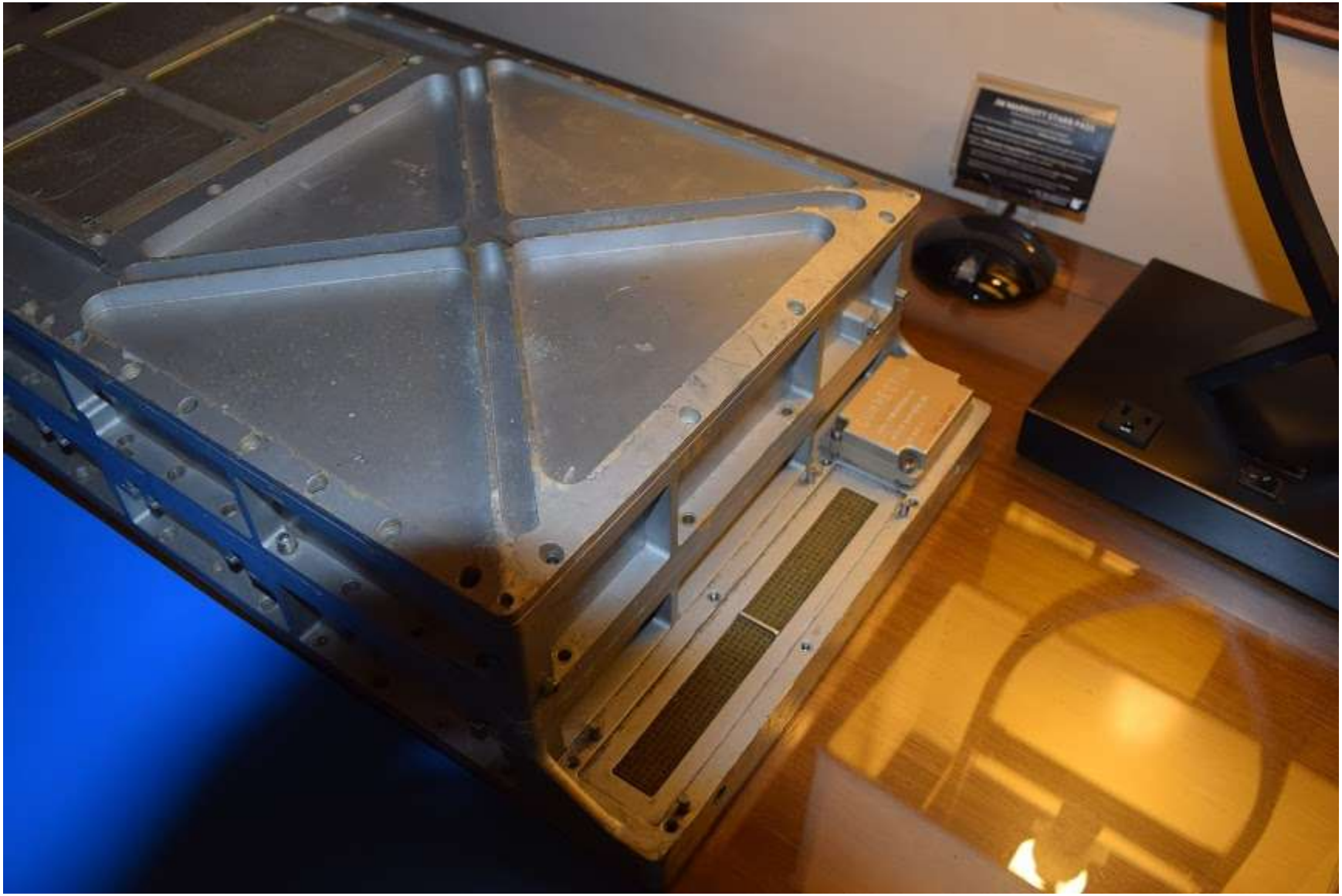
- Developed at MIT, built by Raytheon
- Used on all manned Apollo flights
- Installed in both CM and LM
- Digital autopilot / fly-by-wire
- Navigation
- Guidance
- Control hub for spacecraft
- Primary Guidance, Navigation and Control System - PGNCS or “pings”

AGC quick stats

- 15 bit word, ones complement (mostly[2])
- 1.024MHz clock
- 2K 15 bit words (plus parity) of Eraseable Memory (traditional core 11.96us cycle)
- 36K words of Fixed Memory (ROM) using six core rope modules with 512 cores each

More AGC facts

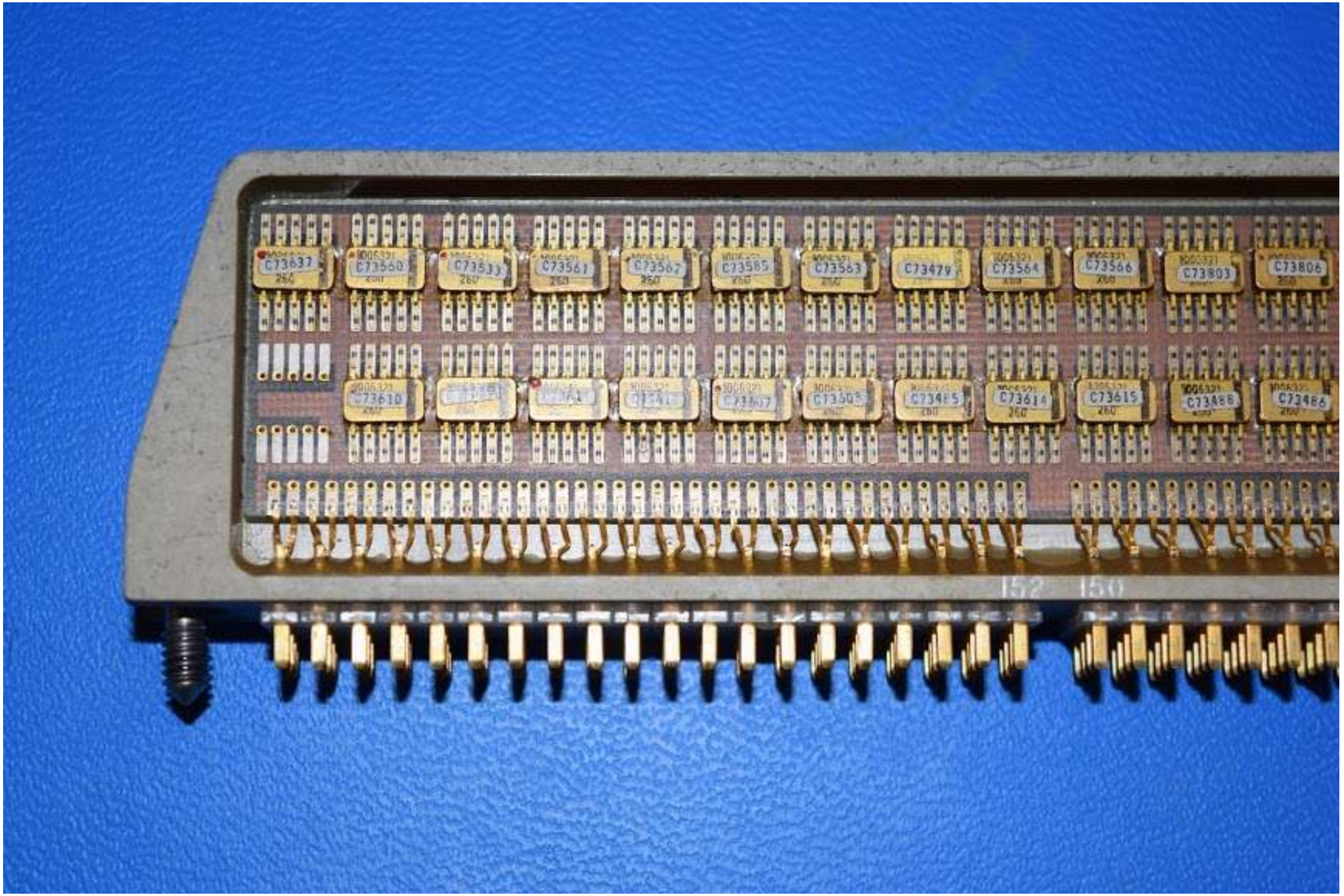
- 3 bit opcode but >170 instructions
- 12 bit memory address = 38K capacity
- Real time, priority operating software
- Checkpoint restart
- Hardware error detection



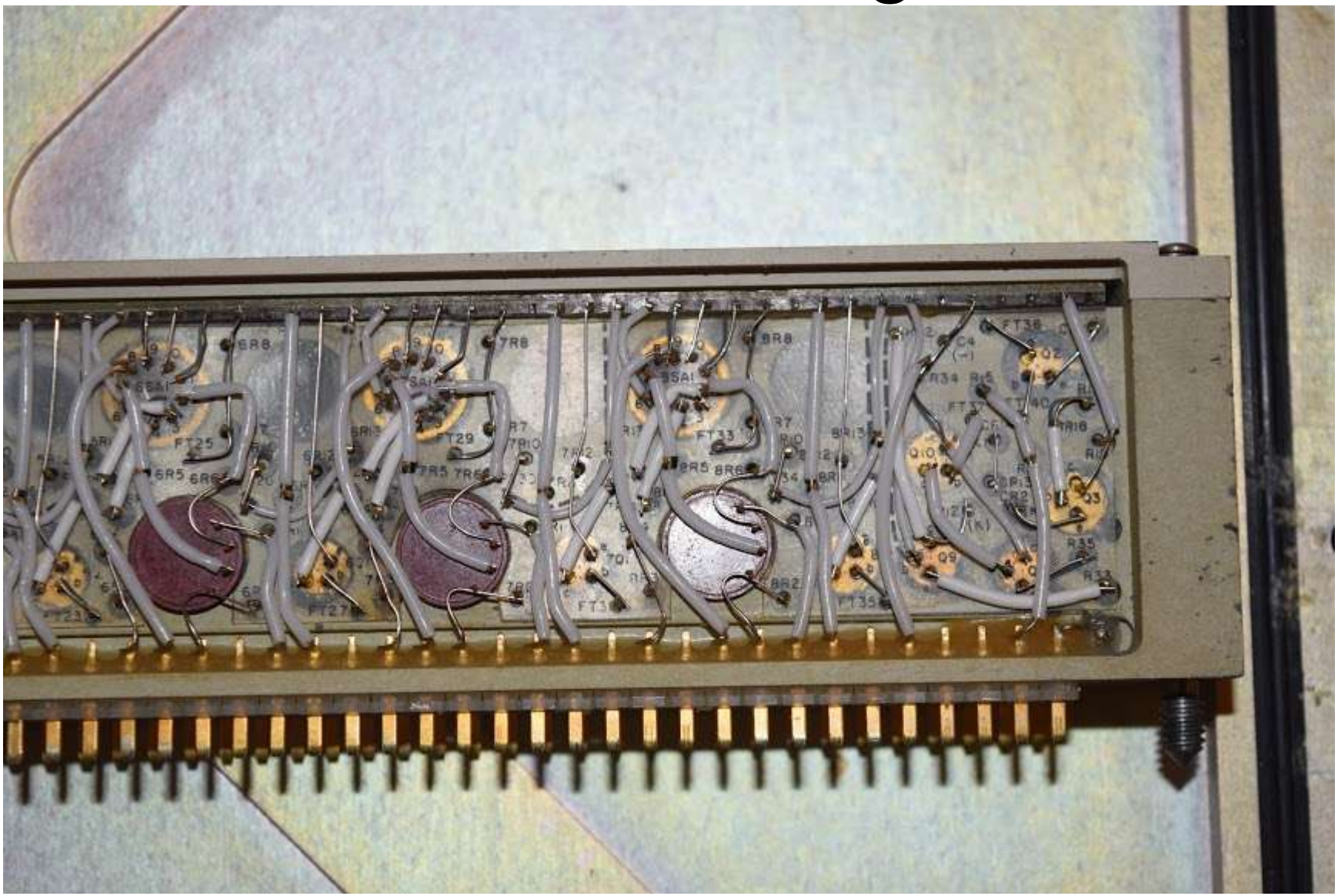
Physical construction

- All logic used dual 3-input NOR gate IC
- Surface mount, welded on 7 layer board
- Two boards per plug-in module
- Two trays (halves), each with modules
- Wire wrap on bottoms of trays

Typical logic module



Cordwood for analog circuits

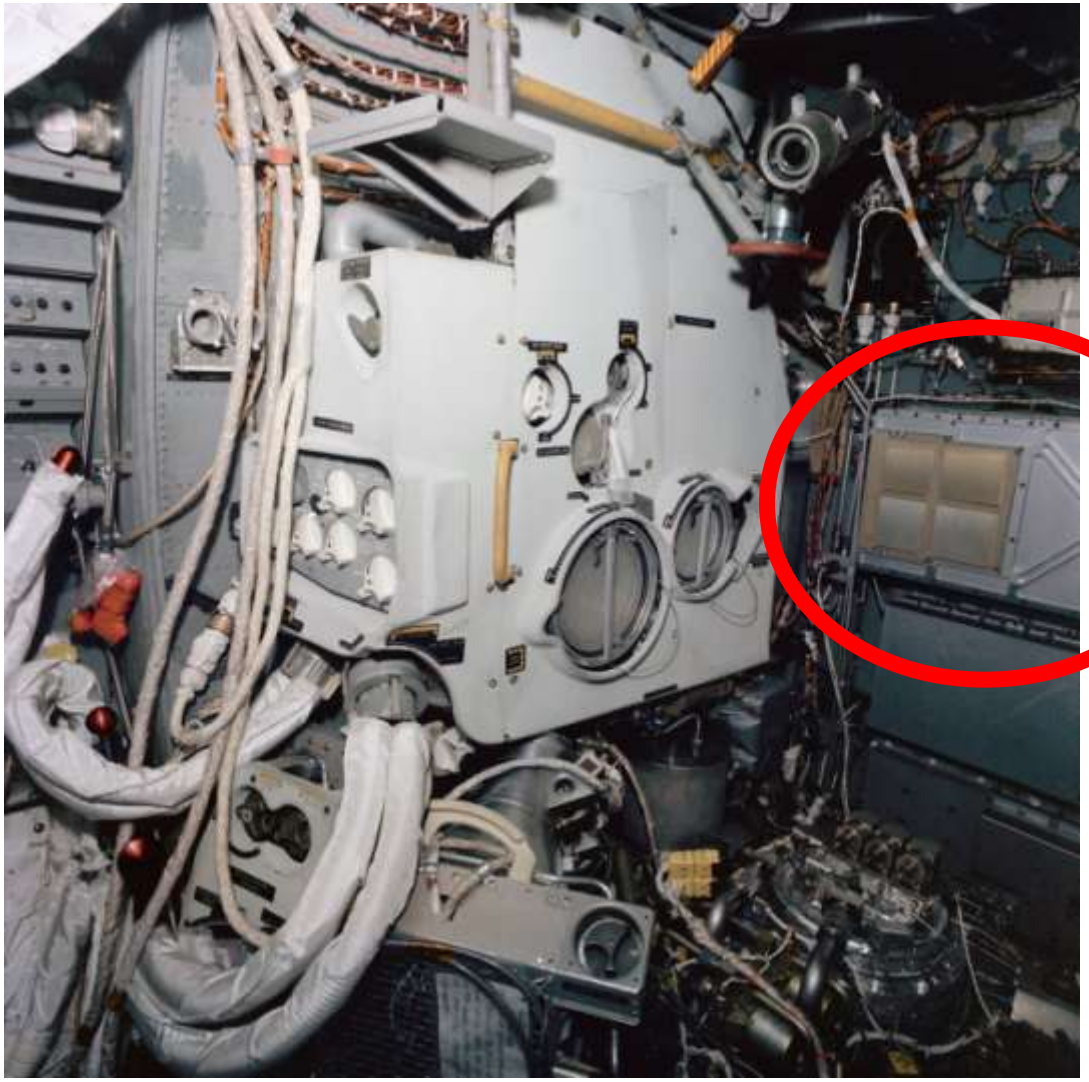



INTERFACE MODULE A27-29
INTERFACE MODULE A27-29
INTERFACE MODULE A27-29
INTERFACE MODULE A25-26
INTERFACE MODULE A25-26
LOGIC MODULE A15
LOGIC MODULE A13
LOGIC MODULE A12
LOGIC MODULE A6
LOGIC MODULE A5
LOGIC MODULE A4
LOGIC MODULE A3
LOGIC MODULE A2
LOGIC MODULE A1

Physical construction

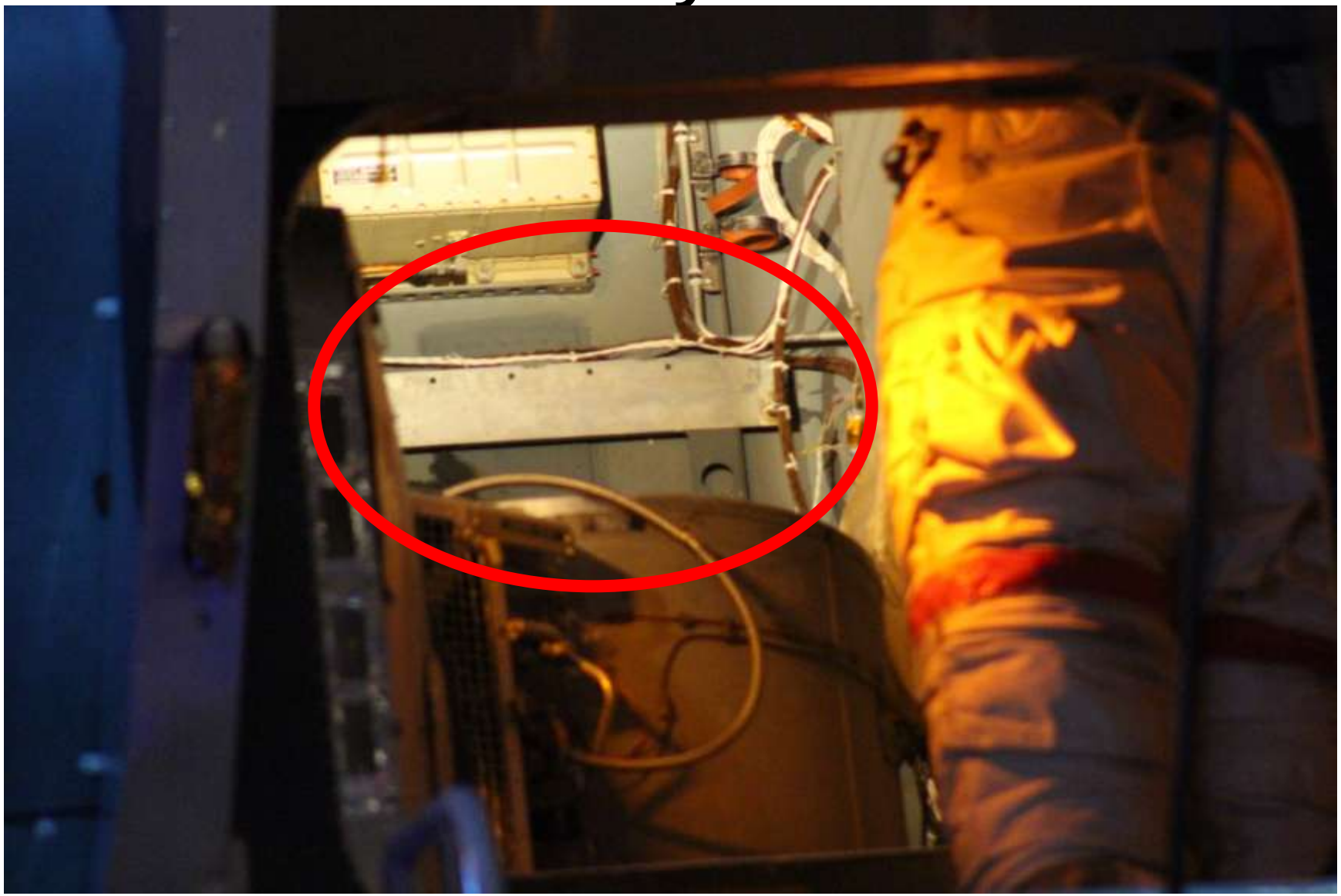
- Unobtainium connectors (Mini-Wasp)
- Second IC type - custom sense amplifier
- Usually potted but not most of #14
- Spacecraft mainly used 28V DC main bus
- Internally generates 14V and 4V

Lunar module Test Article 8



In 1969

LTA-8 today - at JSC



Restoration Team

- Mike Stewart
- Ken Shirriff
- Marc Verdiell
- Carl Claunch

In a hotel room somewhere in Houston . . .

Continuing the restoration

- Reverse engineer core rope simulator and build driver hardware, hosting mission SW
- Build DSKY substitute to communicate
- FPGA based core rope and eraseable memory substitution tool
- Malco mini-WASP pins being produced
- 3D micron resolution X-ray of core module

Core rope simulator modules

DSKY substitute case

DSKY substitute display PCB