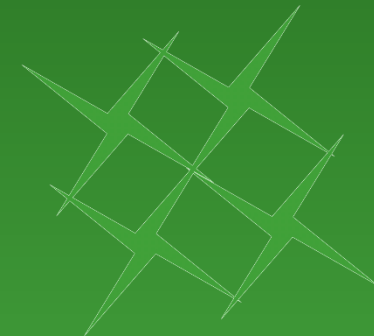




Activities During the Past Year since Forth Day 2018

Greg Bailey
SVFIG Forth Day
16 November 2019



The Past Year

- Orientation with Michael Schuldt
- Create POLYSANCE
- Visit Switzerland: Stefan and Daniel.
- Produce and Ship EVB002
- Release Complete arrayForth 3
- Construct GPS Receiver Demonstration
- Implement GLOW as Operational CAD System
- RIP Bill Muench!



Near Grenchen Switzerland

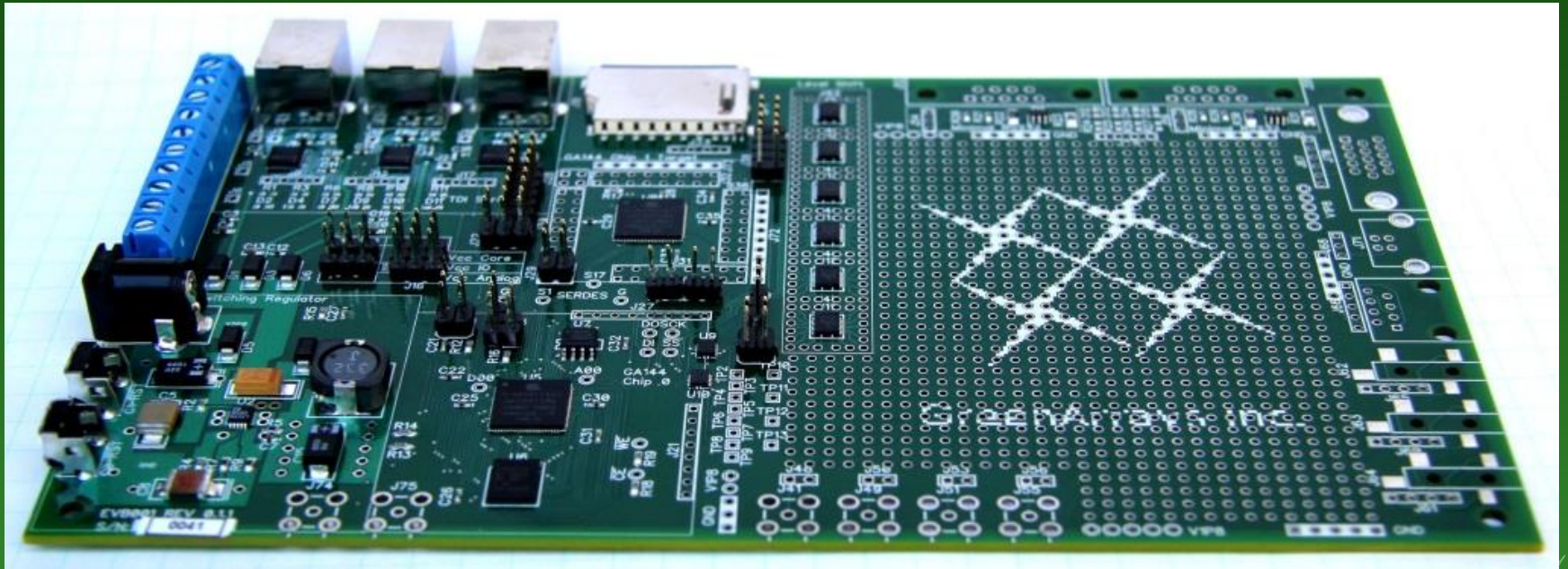


EVB002 Key Changes

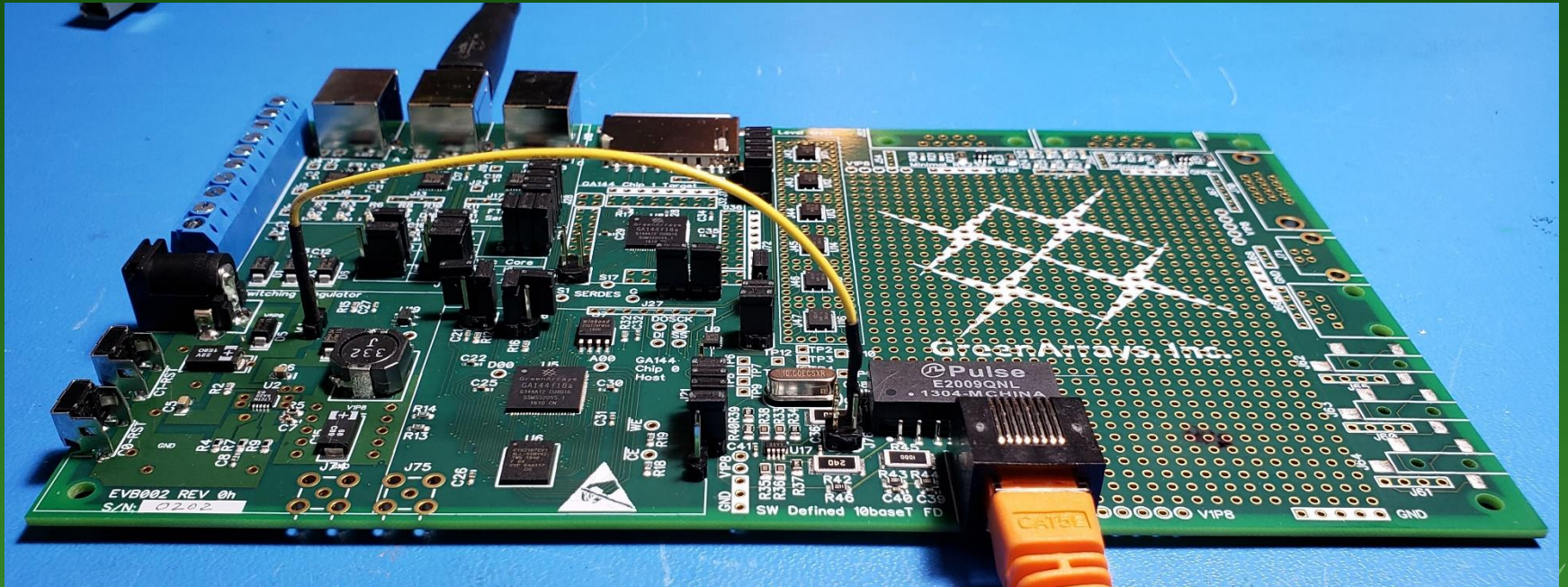
- Increase SPI Flash to 16 MBytes
- Fix small errors in EVB001
 - Power regulator caps; VGA hole pattern; activity LEDs on FTDI USB devices
- Half of level shifters single ended, half push-pull
- Add watchdog/reset chip for optional use
- Add 10baseT interface electronics (xtal, op-amp, magnetics)
- EVB002 may be used as its own development system with external terminal or, later, Telnet.



EVB001 View



EVB002 View



Evaluation Board Reference Manual

for EVB002 rev 0hb
with G144A12 chips

Supported by arrayForth® Version 3

The GreenArrays EVB002 Evaluation Board is a versatile and powerful application development platform for the GA144-1.20 chips. Using arrayForth 3, the EVB002 may serve as a standalone development system with polyFORTH® running on the EVB002 directly, or may be used in conjunction with saneFORTH on x86 platforms. Its many configuration options facilitate intimate, interactive code development at all levels with one or two GA144 chips.

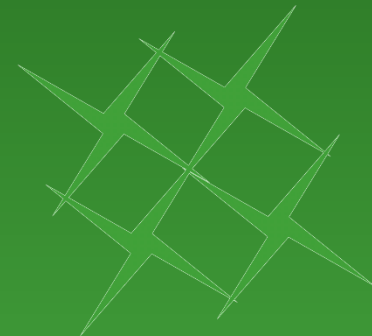
Please familiarize yourself with this information before using the Eval Board so that you will be aware of the many configuration options available to you.

In addition, please download and read the other relevant documentation such as the Programmers' Reference for the F18 computers (DB001), the G144A12 Chip Data Book (DB002), and the User's Manuals DB013 for arrayForth 3, DB005 and DB006 for polyFORTH, and other Application Notes as appropriate. The current editions of all GreenArrays documents, including this one, may be found on our website at <http://www.greenarraychips.com>.

It is always advisable to ensure that you are using the latest documents before starting work.

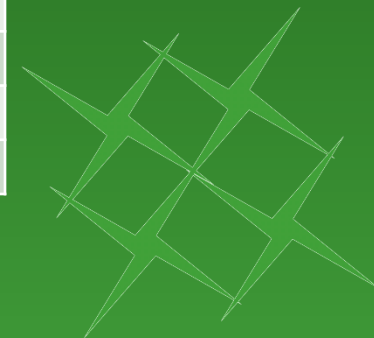
arrayForth 3

- Common syntax and utilities on both saneFORTH/x86 and polyFORTH/144 enable development from host or target systems.
- Existing F18 code, including automated test system, has been converted.
- Improved 2-chip extensible SOFTSIM.



Capabilities of Host and Target

Capability Supported	sF	pF/144
F18 native code Assembler	YES	YES
Source and object code auditing	YES	YES
Concordance and fast FIND in source code	YES	---
Support for 2-chip targets	YES	YES
External IDE	YES	tbd
Internal IDE	---	tbd
Boot stream generation	YES	YES
Boot stream auditing	YES	YES
Internal boot stream delivery (Node 207)	---	YES
Serial boot stream delivery	YES	tbd
Flash boot stream burning in target	tbd	tbd
Flash boot stream burning internal to own system	---	YES
Target Compiler for pF/144 Nucleus	---	YES
Chip test via External IDE	YES	tbd
External SRAM assembly test via external IDE	YES	tbd
ATS Chip Testing	YES	tbd
Software Simulator	BETA	---



```

V      V      V      V      V      V      V      V
302a11 303a11 304a11 305a11 306a11 307a11 308a11 309a11
4f fetch 4f fetch 4f fetch 4f fetch 4f fetch 4f fetch 4f fetch
i115A5 i115A5 i115A5 i115A5 i115A5 i115A5 i115A5 i115A5
>0all< >0all< >0all< >0all< >0all< >0all< >0all< >0all<
a2AAAA a2AAAA a2AAAA a2AAAA a2AAAA a2AAAA a2AAAA a2AAAA
b io b io b io b io b io b io b io b io
o200AA o200AA o200AA o200AA o200AA o200AA o200AA o200AA
r2AAAA r2AAAA r2AAAA r2AAAA r2AAAA r2AAAA r2AAAA r2AAAA
t2AAAA t2AAAA t2AAAA t2AAAA t2AAAA t2AAAA t2AAAA t2AAAA
s2AAAA s2AAAA s2AAAA s2AAAA s2AAAA s2AAAA s2AAAA s2AAAA
^      ^      ^      ^      ^      ^      ^      ^
V      V      V      V      V      V      V      V
202-l- 203-r- 204-l- 205a11 206-r- 207-u- 208a11 209a11
0 @ 0 @ 0 @ 4f fetch 4f fetch 0 @b 4f fetch 4f fetch
i03B40 i03B40 i03B40 i115A5 i00000 i01D93 i115A5 i115A5
>0 21 >0 21 >0 21 >0all< 0-r-< 0 38 >0all< >0all<
a00175 a001D5 a00175 a2AAAA a2AAAA a2AAAA a2AAAA a2AAAA
b -r- b -l- b -u- b -u- b -u- b -u- b io b io
o204AA o204AA o204AA o200AA o204AA o200AA o200AA o200AA
r2AAAA r2AAAA r2AAAA r00002 r2AAAA r2AAAA r2AAAA r2AAAA
t2AAAA t2AAAA t2AAAA t2AAAA t2AAAA t2AAAA t2AAAA t2AAAA
s2AAAA s2AAAA s2AAAA s2AAAA s2AAAA s2AAAA s2AAAA s2AAAA
^      ^      ^      ^      ^      ^      ^      ^
V      V      V      V      V      V      V      V
102-r- 103-l- 104 2E 105-l- 106-r- 107-d- 108-l- 109-r-
0 @ 0 @ 4f fetch 1 !b 2 @b 2 @b 0 @b 0 @b
i03B40 i03B40 i1B424 i05B05 i09B05 i09B02 i01A55 i01A55
0 21< 0 21< 1 2F 0 04> 0 3E< 0 1A >0 07 >0 11
a001D5 a00175 a001D5 a001D5 a2AAAA a001D5 a001D5 a00175
b -l- b -r- b io b -l- b -r- b -d- b -l- b -r-
o204AA o204AA o304AA o378AA o27CAA o200AA o240AA o250AA
r2AAAA r2AAAA r2AAAA r00032 r00175 r0001C r001D5 r00175
t2AAAA t2AAAA t20954 t011DC t00000 t20000 t2AAAA t2AAAA
s2AAAA s2AAAA s012A8 s00002 s00000 s15555 s2AAAA s2AAAA
^      ^      ^      ^      ^      ^      ^      ^
V      V      V      ^      ^      +ph 0010 +ph
002rd1 003rd1 004rd1 005-d- 006-d- 007 40 008r-1 009-r-
4f fetch 4f fetch 4f fetch 1 !b 1 !b 0unext 0 @b 0 @b
i115B5 i115B5 i115B5 i05B40 i05B40 i1DB0A i01A8A i004DA
>0rd1< >0rd1< >0rd1< 0 03 0 03 0 41 >0 25< >0 27
a2AAAA a2AAAA a2AAAA a2AAAA a2AAAA a00141 a0015D a00141
b io b io b io b -d- b -d- b -l- b r-1 b -r-
o202AA o202AA o202AA o272AA o372AA o102AA o04291 o052AA
r2AAAA r2AAAA r2AAAA r2AAAA r2AAAA r0001D r2AAAA r2AAAA
t2AAAA t2AAAA t2AAAA t2AAAA t2AAAA t3557F t2AAAA t00003
s2AAAA s2AAAA s2AAAA s2AAAA s2AAAA s00141 s2AAAA s2AAAA
00E1F 04770

```

```

00008 p= 25 io=04291 b=r-1 a=0015D io
pins= 0010 data=
>.< i=01A8A @b ! a . 2AAAA
loc= 24 slot=0 @b 2AAAA
SUSPENDED 2AAAA
1D 134A9 call A9 2AAAA
1E 134A9 call A9 2AAAA
1F 134A9 call A9 2AAAA
start 20 04B12 @p b! @p . 2AAAA
21 001F5 @b + + ; r2AAAA
22 0015D @b + ex ;
23 2A9B2 a! . . . t2AAAA
cmd 24 01A8A @b ! a . s2AAAA
25 2FDB2 >r @p . . 2AAAA
26 00007 @b and @b @p 2AAAA
27 01B03 @b !b @b dup 2AAAA
28 087C2 !b 2/ 2/ . 2AAAA
29 3EAB2 and a! . . 2AAAA
2A 02CAA @ r> a! . 00007
2B 0B724 ! jump 24 2AAAA
last 2C 134A9 call A9 2AAAA

```

SOFTSIM Help for sF/Win32 System

OVIEW	Use IJKL keys to reposition overview rectangle.
nn SEE	Select node nn (cyyxx) for focus node view.
OTHER	Switch to previous focus node view.
a MEM	Start memory display at a and lock it until -MEM
a s nn BREAK	Set node nn breakpoint at adr a slot s.
nn -BREAK	Clear any breakpoint for node nn.
SS	Single step on each keystroke, punch out on ENTER.
n SUPER	n Steps without disp update. FAST updates "time".

ok

-

arrayForth® 3 User's Manual

Rev 03b5+ for G144A12 chips

*Running on saneFORTH™/Win32
and polyFORTH® for GA144*

This manual is designed to prepare you for using arrayForth 3 (aF-3) in designing, implementing and testing applications of our chips.

aF-3 is a complete, interactive software development , debugging and installation environment for GreenArrays Chips. It includes an F18 Assembler, example source code including all ROM on each chip, a full software-level simulator for each chip, an Interactive Development Environment for use with real chips, and utilities for creating boot streams and burning them into flash memory. As of aF-3, colorForth is no longer used in this system.

aF-3 is written to run on polyFORTH in G144A12 environments with sufficient resources, and on saneForth for Win32 environments. These versions complement each other and each has a different emphasis of tools, reflecting their differing purposes. The principal purpose of the Win32 environment is cross-compiling for new chips, commission new boards, and simulate at high speeds. The G144A12 environment is intended for interactive development and testing, with F18 and polyFORTH source code in a single base that can be maintained by either system. In most cases, we intend that you will be using an EVB instead of a PC as the principal host for software development.

Although it is configured to support the GreenArrays EVB002 Evaluation Board, it may easily be used to program and debug our chips on the EVB001 in your own designs.

Along with the above tools, including complete source code for the Virtual Machine environments, this release incorporates the source code for our Automated Testing systems as well as that which has been used in taking the characterization measurements reflected in the G144A12 Data Book.

Your satisfaction is very important to us! Please familiarize yourself with our Customer Support web page at <http://www.greenarraychips.com/home/support>. This will lead you to the latest software and documentation as well as resources for solving problems and contact information for obtaining help or information in real time.

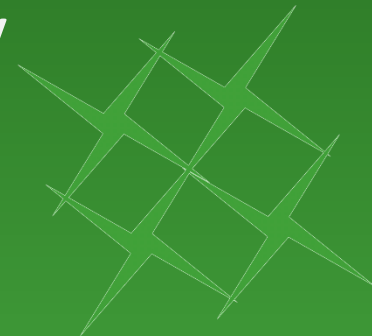
GPS Receiver Demonstration

- Why? Customer wishes to minimize overall energy per fix. 24 hour battery life completely unacceptable.
- Initial Work in June 2013
- Preparation for Demo started Dec 2018
 - SoftOSGPS (Cliff Kelley) on Sourceforge with test data and “correct” results
- Search for *suitable* RF front end chips, both available and documented, took until June 2019
- Intensive work during July and September 2019



Nature of the Signal

- All 32 satellites broadcast signal on same carrier frequency ~ 2 GHz. A subset visible at any time.
- Each signal AM'd with a 1023-bit PRN for each satellite, at 1.023 MHz (one PRN per ms).
- Message data bits encoded at 50 b/sec by inverting, or not, 20 consecutive PRNs (20 ms) per bit. One frame is 1500 bits, full message is 25 frames (37500 bits, 12.5 minutes)
- Signals (including modulation) affected by Doppler, Ionosphere, etc.



Low Level Problem Statement

- Receive 2-bit samples from IF ADC at $\sim 5\text{MHz}$
- Compute and sum four correlations on each sample for each of 12 satellites every $\sim 200\text{ ns}$
- Inject revised phase angle increments into, and receive correlation sums from, all correlators every 1 ms.
- Run low level control loops for acquisition and tracking to provide new phase increments
- Provide mechanism to configure correlators for new satellites
- Time critical in the sense that we must not drop any incoming samples.

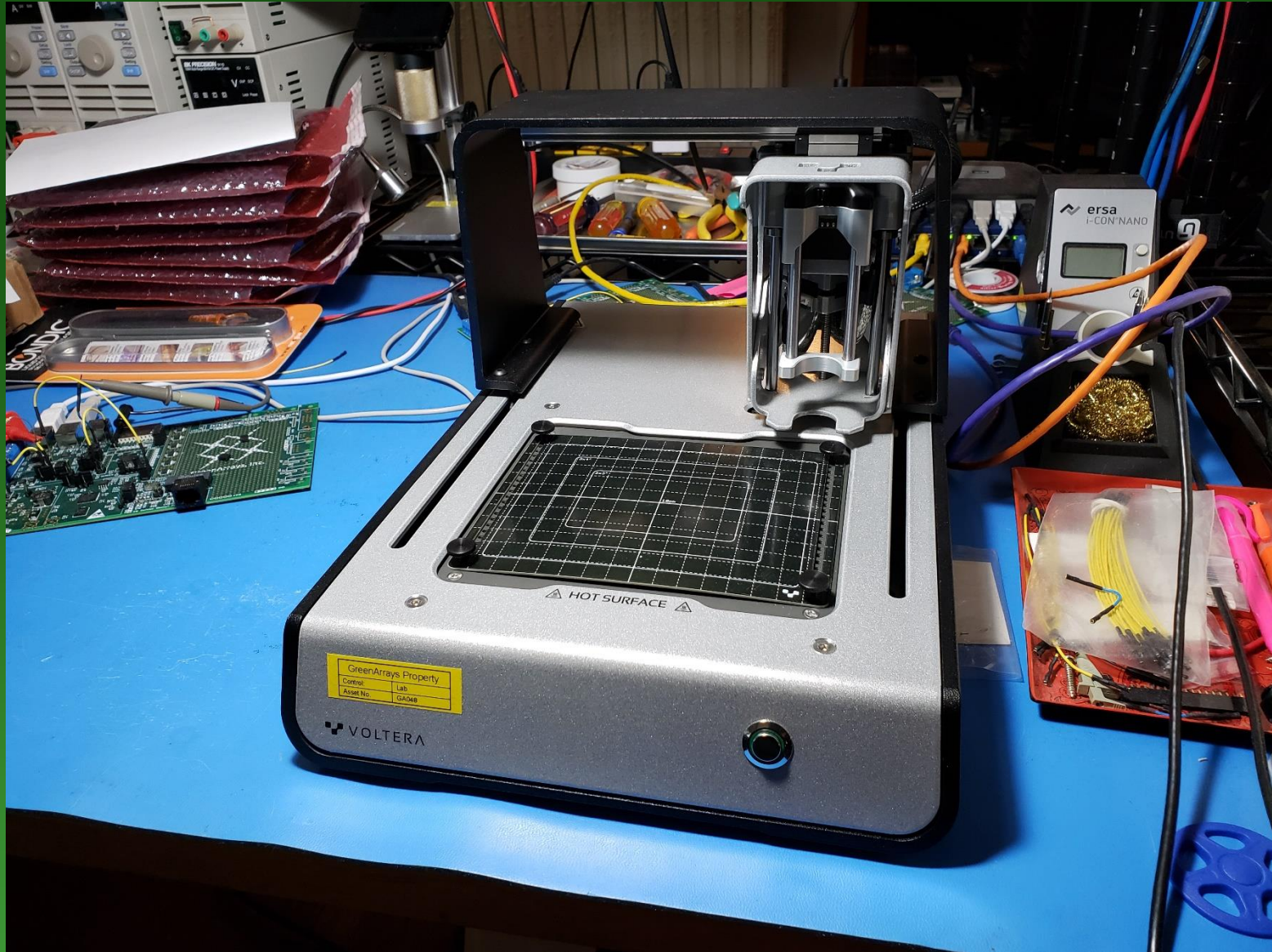


High Level Architecture

- All of the time critical parts of the 1 ms cycle implemented in F18 nodes with native code
- High level functions (such as message parsing, retrieving and storing almanac and orbital elements, computing ephemerides, deriving time and position) done in high level polyFORTH.
- Current design inhabits a single G144A12 with external SPI flash, external SRAM, and external RF front end chip.

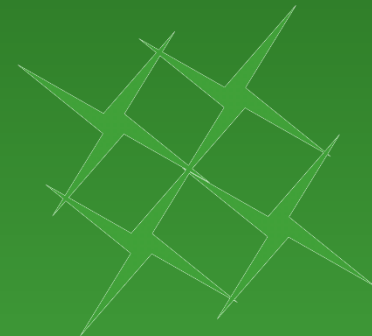


Voltera™ Rapid PCB Manufacture



For More Information on GreenArrays and These Projects

- Primary Website
 - <http://www.greenarraychips.com>
 - Get all documents here
- Announcement Blog
 - Technical <http://www.greenarraychips.com/blog2>
- Tech Support on e-mail, Skype, Phone





Thank You!

For more information, please visit
<http://www.greenarraychips.com>

