

Forth Day 2013



Topics

- Forth-2012 Public Review RC2
- MACH 2 Anyone?
- Atmel SAM4S Flash Programming
- Forty Years of FORTH, Inc.



Forth-2012 Public Review

- The second release candidate draft of the proposed Forth 2012 standard is now available for public review from the Forth200x web site and from the FORTH, Inc. web site.
- Final review period is three months.
- Submit comments to Forth200x Group.
- Details on forth.com home page (left sidebar, “Forth Standard Review RC2”)



SwiftX Interactive Development



SwiftX Cross-Target Link (XTL)

- Read memory
- Write memory
- Read registers
- Write registers
- Download code
- Remote execution
- Program flash



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Flash Programming

```
LABEL FLASHLOADER
  CPSID                                \ Disable interrupts
  EEFC0_BASE R2 LDRI  UART_XTL R3 LDRI \ Flash controller and UART base addr
  |CODE| |EPA| 1- + |EPA| / R4 MOVS    \ Number of 16-page erase commands
  5A000307 R5 LDRI  BEGIN              \ Erase 16 pages command (start page 0)
  EEFC0_FCR R2 R5 STR                  \ Erase pages
  BEGIN  EEFC0_FSR R2 R0 LDR           \ Poll flash status
  1 R0 R0 LSRS  CS UNTIL               \ ...until done
  2000 R0 LDRI  R0 R5 R5 ADDS          \ Bump to next chunk of pages
  1 R4 R4 SUBS  0= UNTIL
  0 R0 MOVS  <XMT> BL
  #FPAGES R4 LDRI  5A000001 R5 LDRI    \ Page count, page# with write page command
  BEGIN  |FPAGE| R6 LDRI  'FLASH R7 LDRI
  BEGIN  <RCV> BL  0 R7 R0 STR        \ Receive flash block into flash page buffer
  4 R7 R7 ADDS  4 R6 R6 SUBS  0= UNTIL \ ...in cell units
  EEFC0_FCR R2 R5 STR                  \ Issue page write command for this page
  100 R0 LDRI  R0 R5 R5 ADDS           \ Bump page# for next time
  BEGIN  EEFC0_FSR R2 R0 LDR           \ Poll flash status
  1 R0 R0 LSRS  CS UNTIL               \ ...until done
  0 R0 MOVS  <XMT> BL
  1 R4 R4 SUBS  0= UNTIL
  <ACK> R0 MOVS  <XMT> BL
  RSTC_BASE R1 LDRI  A5000005 R0 LDRI  \ Reset processor and peripherals
  RSTC_CR R1 R0 STR  END-CODE
```



Only Erase What You Need

```
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  CPSID                                \ Disable interrupts
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  |CODE| |EPA| 1- + |EPA| / R4 MOVS      \ Number of 16-page erase commands
  5A000307 R5 LDRI   BEGIN              \ Erase 16 pages command (start page 0)
  EEFC0_FCR R2 R5 STR                   \ Erase pages
  BEGIN EEFC0_FSR R2 R0 LDR             \ Poll flash status
  1 R0 R0 LSRS   CS UNTIL               \ ...until done
  2000 R0 LDRI   R0 R5 R5 ADDS          \ Bump to next chunk of pages
  1 R4 R4 SUBS   0= UNTIL
  0 R0 MOVS     <XMT> BL
  #FPAGES R4 LDRI   5A000001 R5 LDRI    \ Send result=0
  BEGIN |FPAGE| R6 LDRI   'FLASH R7 LDRI \ Page count, page# with write page command
  BEGIN <RCV> BL   0 R7 R0 STR         \ Receive flash block into flash page buffer
  4 R7 R7 ADDS   4 R6 R6 SUBS   0= UNTIL \ ...in cell units
  EEFC0_FCR R2 R5 STR                   \ Issue page write command for this page
  100 R0 LDRI   R0 R5 R5 ADDS          \ Bump page# for next time
  BEGIN EEFC0_FSR R2 R0 LDR             \ Poll flash status
  1 R0 R0 LSRS   CS UNTIL               \ ...until done
  0 R0 MOVS     <XMT> BL                 \ Send ior=0 for page load
  1 R4 R4 SUBS   0= UNTIL                \ Loop until all pages programmed
  <ACK> R0 MOVS  <XMT> BL                 \ Send <ack> for successful download
  RSTC_BASE R1 LDRI   A5000005 R0 LDRI  \ Reset processor and peripherals
  RSTC_CR R1 R0 STR   END-CODE
```



Program in Pages

```
LABEL FLASHLOADER
  CPSID                                \ Disable interrupts
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  1 R4 R4 SUBS  0= UNTIL
  0 R0 MOVS  <XMT> BL
  #FPAGES R4 LDRI  5A000001 R5 LDRI    \ Page count, page# with write page command
  BEGIN  |FPAGE| R6 LDRI  'FLASH R7 LDRI
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  EEFC0_FCR R2 R5 STR                  \ Issue page write command for this page
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  BEGIN  EEFC0_FSR R2 R0 LDR           \ Poll flash status
  1 R0 R0 LSRS  CS UNTIL               \ ...until done
  0 R0 MOVS  <XMT> BL                  \ Send ior=0 for page load
  1 R4 R4 SUBS  0= UNTIL               \ Loop until all pages programmed
  <ACK> R0 MOVS  <XMT> BL              \ Send <ack> for successful download
  RSTC_BASE R1 LDRI  A5000005 R0 LDRI \ Reset processor and peripherals
  RSTC_CR R1 R0 STR  END-CODE
```



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