eP32 for Lattice Brevia Kit

Silicon Valley FIG

Forth Day

11/20/2010

Chen-Hanson Ting


LatticeXP2 Brevia
Development Kit
YOUR TICKET TO RAPID DESIGN
Lattice
Now Only
$49
Order Today

LatticeXP2 Brevia Kit

The Most Satisfying FPGA

- I have tried FPGA's from all Big 4:

	Market Share	2009 Sales	FPGA
Xilinx	50%	$1,825M	Virtex, Spartan
Altera	30%	$360M	Stratix, Cyclone
Lattice	10%	$194M	ECP3, XP2
Actel	6%	$190M	IGLOO, ProASI

- Lattice has the most satisfying FPGA, a single chip SOC solution
- Lattice had the cheapest development board. $49
- Lattice has the cheapest development software. Free

LatticeXP2 Brevia Kit

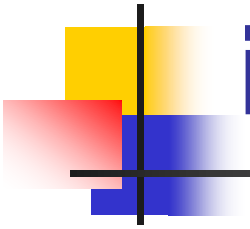
- LatticeXP2-5E 6TN144C
- 2-Mbit SPI Flash memory
- 128K by 8-bit SRAM
- RS232 DB9 connector
- 8 Switches/Pushbuttons
- Reset pushbutton
- 8 status LEDs
- JTAG Interface
- Parallel Port ispDownload Cable

LatticeXP2-5E 6TN144C

- 5K LUT4 Logic cells
- 166K Bits Embedded block memory
- 10K Bits Distributed memory
- 3 DSP Blocks
- 12 18x18 Multipliers
- 2 PLL
- 144 Pin TQFP Package

ispLEVER Design Software

- ispLEVEL Starter for Windows
- Synplify Synthesis Tool
- Aldec Active-HDL Simulator
- ispVMR FPGA Programmer
- XP2 Brevia SOC Demo
- LatticeMico8 Reference Design
- Many other reference designs

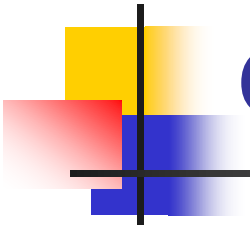


ispLEVER Design Flow

- Verilog/VHDL Design Entry
- Synplify Synthesis
- Functional Simulation
- Design Planner
- Place and Route
- Timing Analysis
- FPGA Programming

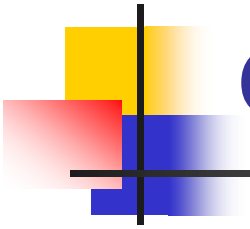
Comments on ispLEVER

- Extremely complex
- Require 5 GB disk space
- Starter system only does functional simulation
- LatticeMico8 is very complicated
- LatticeXP2-5E is very capable and pleasant



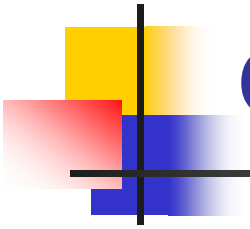
eP32 on LatticeXP2-5E

- Logic design is stored in Flash
- EBR RAM is mirrored in Flash
- 166 Kbits (5K 32-bit Words) are enough to host eForth
- External memories are not necessary
- Speed 50 MHz without much effort
- May be pushed to 200 MHz



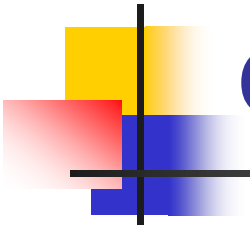
eP32 on LatticeXP2-5E

- eP32_chip.vhd, top level design
- Modules
  - eP32.vhd, CPU core
  - Ram_memory.vhd, 4096x32 RAM memory
  - Uart.vhd, 115200 baud
  - Gpio.vhd, 16 bit bidirectional



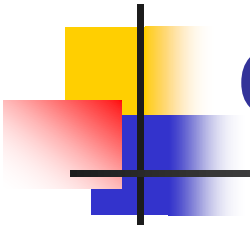
eP32 on LatticeXP2-5E

- Transfer Instructions
  - CALL, BRA, BZ, BC, RET, NEXT
- Memory Instructions
  - LDX, STX, LDXP, STXP, LDI
- Arithmetic Instructions
  - COM, SHL, SHR, AND, XOR, ADD, MUL, DIV, RR8
- Register and Stack Instructions
  - PUSHS, POPS, PUSHR, POPR, TX, XT, OVER, DROP, NOP



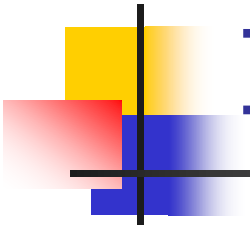
eP32 on LatticeXP2-5E

- 1115 Logic Slices (47%)
- 8 out of 9 EBR memory blocks (89%)
- 54 MHz clock max



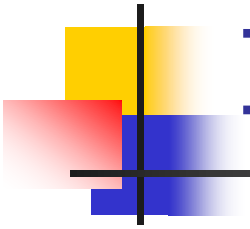
eForth on LatticeXP2-5E

- 175 Words
- 32 Bit program and data words
- Each word contains 1-5 machine instructions
- 50 MHz execution rate
- No byte addressability
- Initialized from flash memory to RAM



Implementation

- Ep32.vhd, uart.vhd and gpio.vhd compiled without modification
- Ram_memory.vhd was pulled from IPexpress
- Ep32_chip.vhd instantiates new ram_memory.vhd
- IO pins assigned using Design Planner
- Test bench constructed for simulation

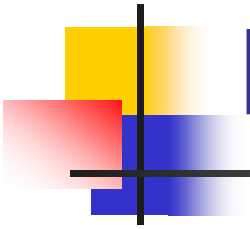


Implementation

- Synthesis went smoothly
- Simulation worked only after test bench was constructed correctly
- ispDownload cable had a broken wire inside
- RESET button still does not work. To restart, cycle power.

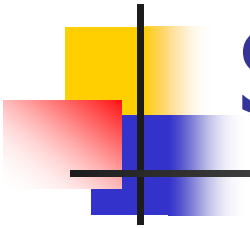
ispDownLoad Cable

- Uses Parallel Port on PC for JTAG interface
- Supports almost every device with JTAG boundary scan
- Uses ispVM System to download and program devices



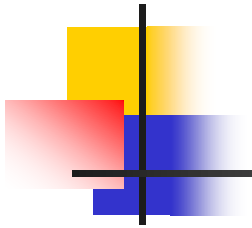
Demo

- FPGA programming cannot be shown because ispDownload cable requires a parallel port on PC.
- Power up Brevia Kit and it talks to HyperTerminal on PC.
- Turn LED's on and off
- Read pushbutton switches

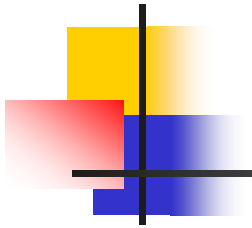


Summary

- Lattice Brevia Board has eP32 now.
- LatticeXP2 is the best, through not the largest or fastest, FPGA for single chip SOC applications.
- ispDownLoad cable is the best JTAG programmer I have seen so far.



Questions?



Thank You.