

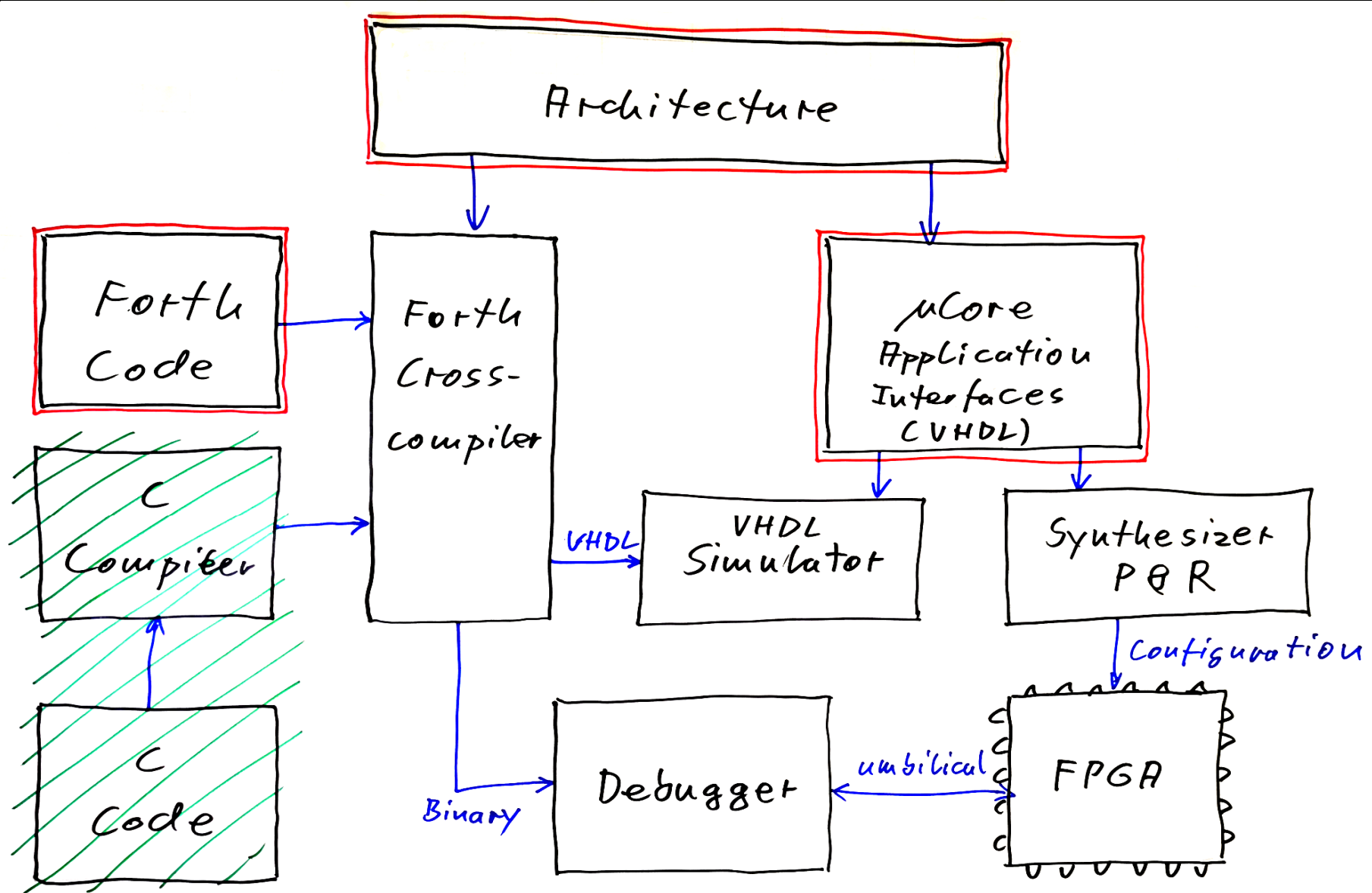
μ Core

VHDL Code
and Structure

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Design Flow



VHDL Interpreter

Forth definitions

```
' \ Alias -- immediate

: base>number ( addr len -- n ) over c@
  [char] ' case? IF 1 /string drop c@ [char] 1 =          EXIT THEN
  [char] " case? IF 1 /string [char] " token binary s>number drop EXIT THEN
  [char] 0 case? IF 1 /string [char] " token octal s>number drop EXIT THEN
  [char] X = IF 1 /string [char] " token hex s>number drop EXIT THEN
  2dup [char] # scan dup                                \ is it a NATURAL with base prefix?
  IF 2>r [char] # token decimal s>number drop Base !
  2r> [char] # token s>number drop
  EXIT THEN 2drop                                       \ its a decimal number
  BL token decimal s>number drop
;
: VHDL-number ( <source> -- n ) Base save BL skip-input [char] ; parse base>number ;
: dec_parameter ( <source> -- n ) Base save BL skip-input [char] ; parse decimal s>number drop ;

Vocabulary --VHDL --VHDL definitions

1 Constant STD_LOGIC
1 Constant byte
1 Constant NATURAL
1 Constant INTEGER
2 Constant BOOLEAN
3 Constant REAL

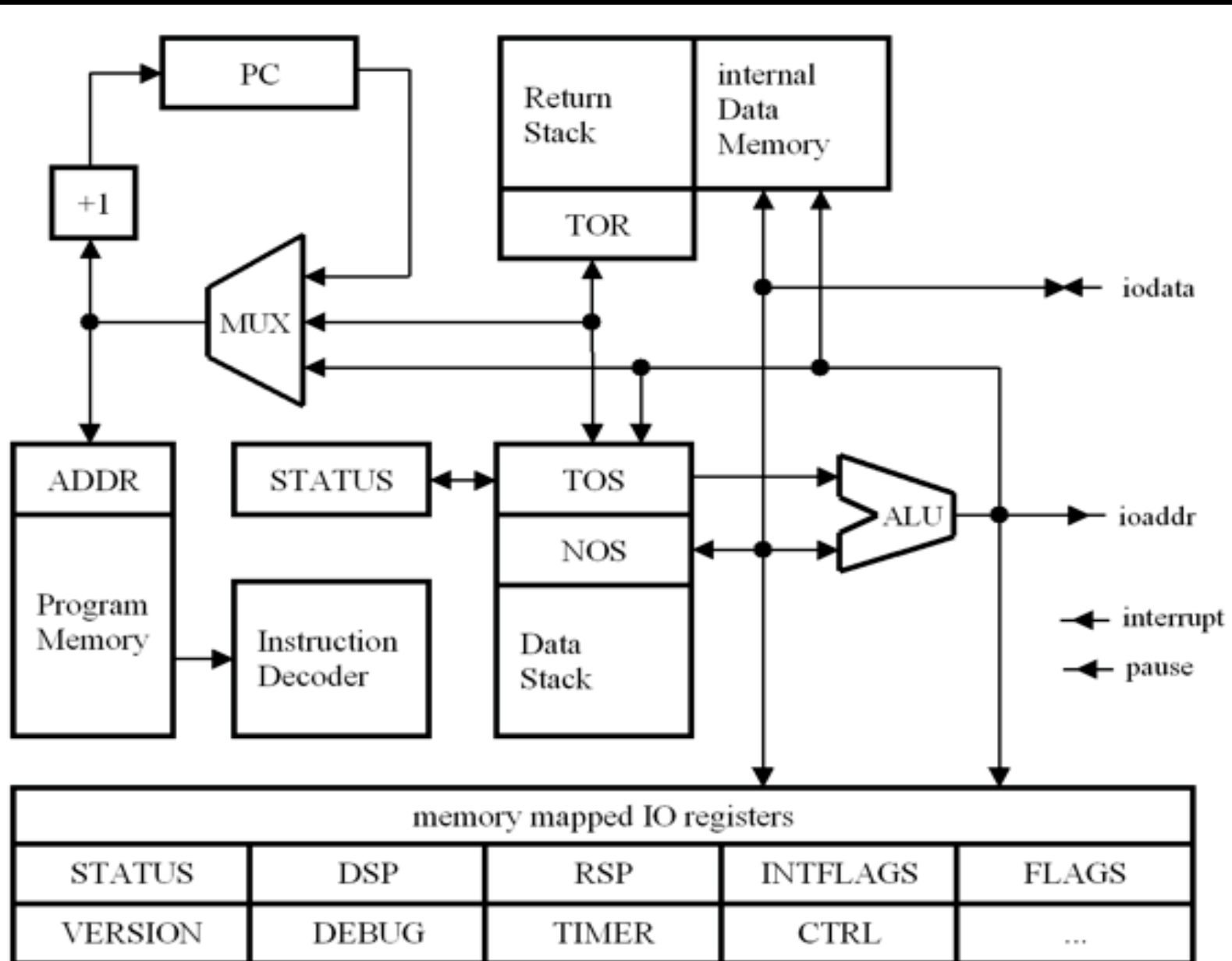
: STD_LOGIC_VECTOR ( -- type ) postpone ( byte ; \ )
: UNSIGNED ( -- type ) postpone ( byte ; \ )

: CONSTANT ( -- ) 0 Constant ;

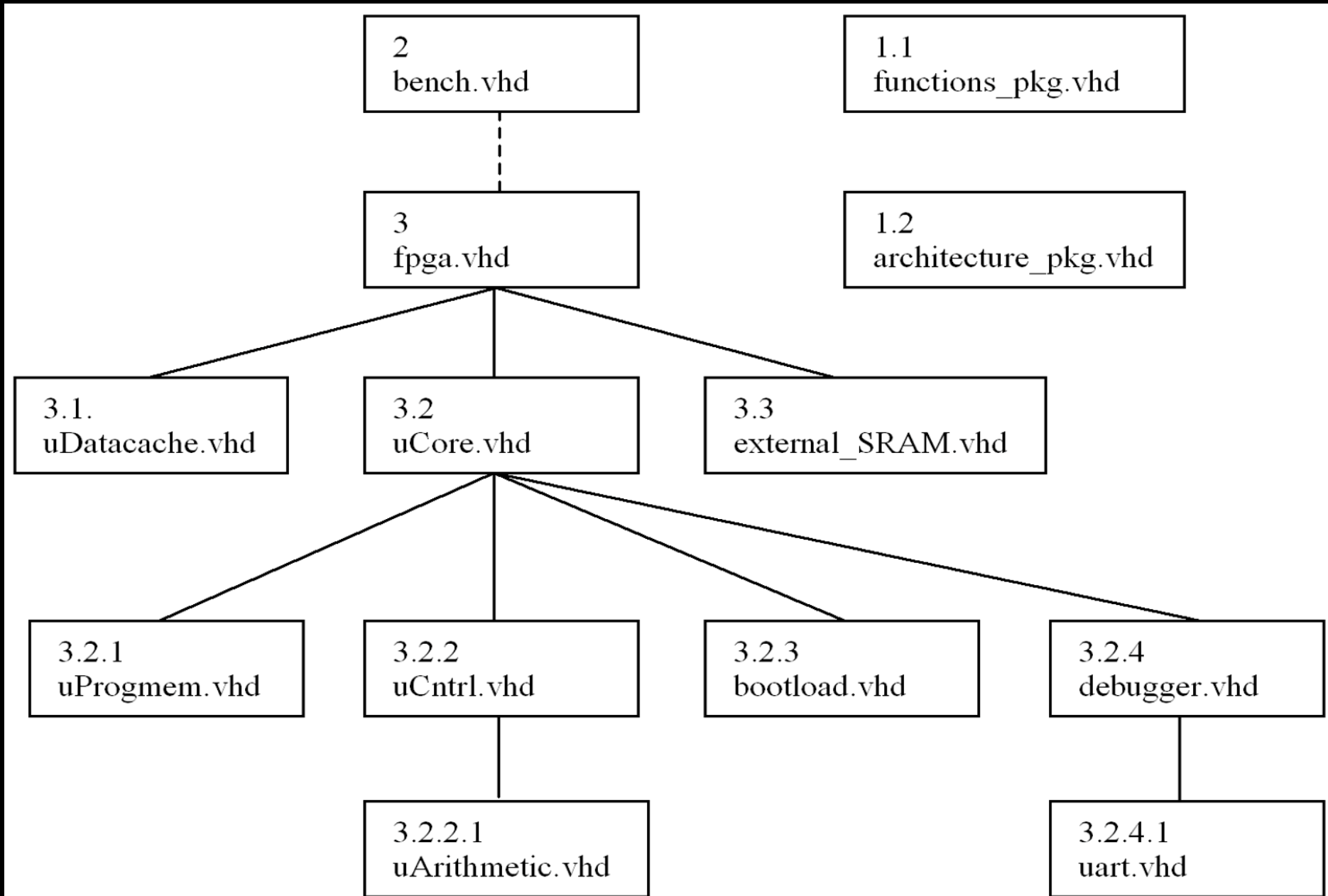
: vhd1-types ( type -- n )
  1 case? IF VHDL-number          EXIT THEN
  2 case? IF [char] ; word count evaluate EXIT THEN \ for conditional compilation
  3 case? IF dec_parameter &10 /  EXIT THEN
  abort" unknown type"
;
: := ( type -- ) Base save vhd1-types here cell- ! ; \ patch constant created before
: --~ ( ccc~ -- ) [char] ~ scan-input ; \ ~
: --Forth ( ccc~ -- ) Forth --~ ;

' \ Alias --
' noop Alias ;
' noop Alias ;
```

Architecture

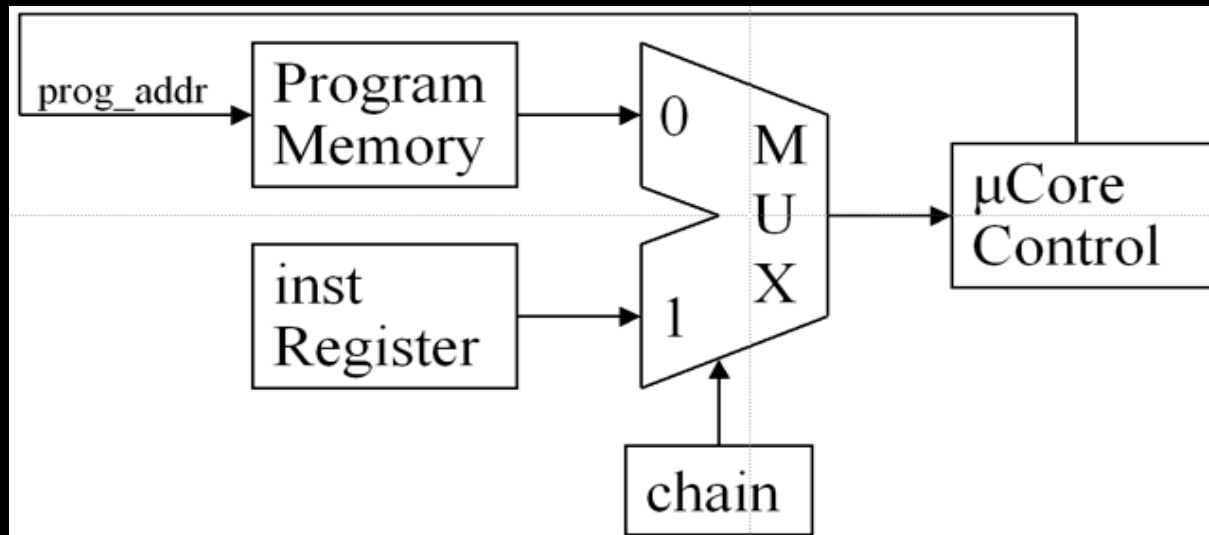


VHDL Structure



2 Cycle Instructions

instruction	2 nd cycle
r>	store memory data into TOR
rdrop	store memory data into TOR
exit, iret	store memory data into TOR
?exit	only executed when TOS \neq 0: store memory data into TOR
next	only executed when finishing a FOR ... NEXT loop (TOR = 0): store memory data into TOR
@	store memory data into TOS
+!	write (memory data + NOS) back into memory
I	store the sum of TOR and data memory (2 nd return stack item) into TOS
IF	in the 1 st cycle, the branch address is dropped, in the 2 nd cycle the flag as well



Instantiations

- μ Core has been ported to Xilinx (**XC2S**), Lattice (**XP2**), Altera (**EP2**), and Actel/Microsemi (**A3PE**) FPGAs.
- Reference instantiations using an **LFXP2-8**:

Instruction set	word width	SLICES	data memory	program memory	maximum clock
core	16	988	6k	8k	33 MHz
extended	16	1199	6k	8k	30 MHz
core	27	1259	4k	8k	33 MHz
extended	27	1608	4k	8k	28 MHz
extended and floating point	27	1808	4k	8k	26 MHz
core	32	1432	3k	8k	33 MHz

Links

microCore is available on git:

<https://github.com/microCore-VHDL>

and here is documentation:

<https://github.com/microCore-VHDL/microCore/tree/master/documents>