µCore

VHDL Code and Structure part 2

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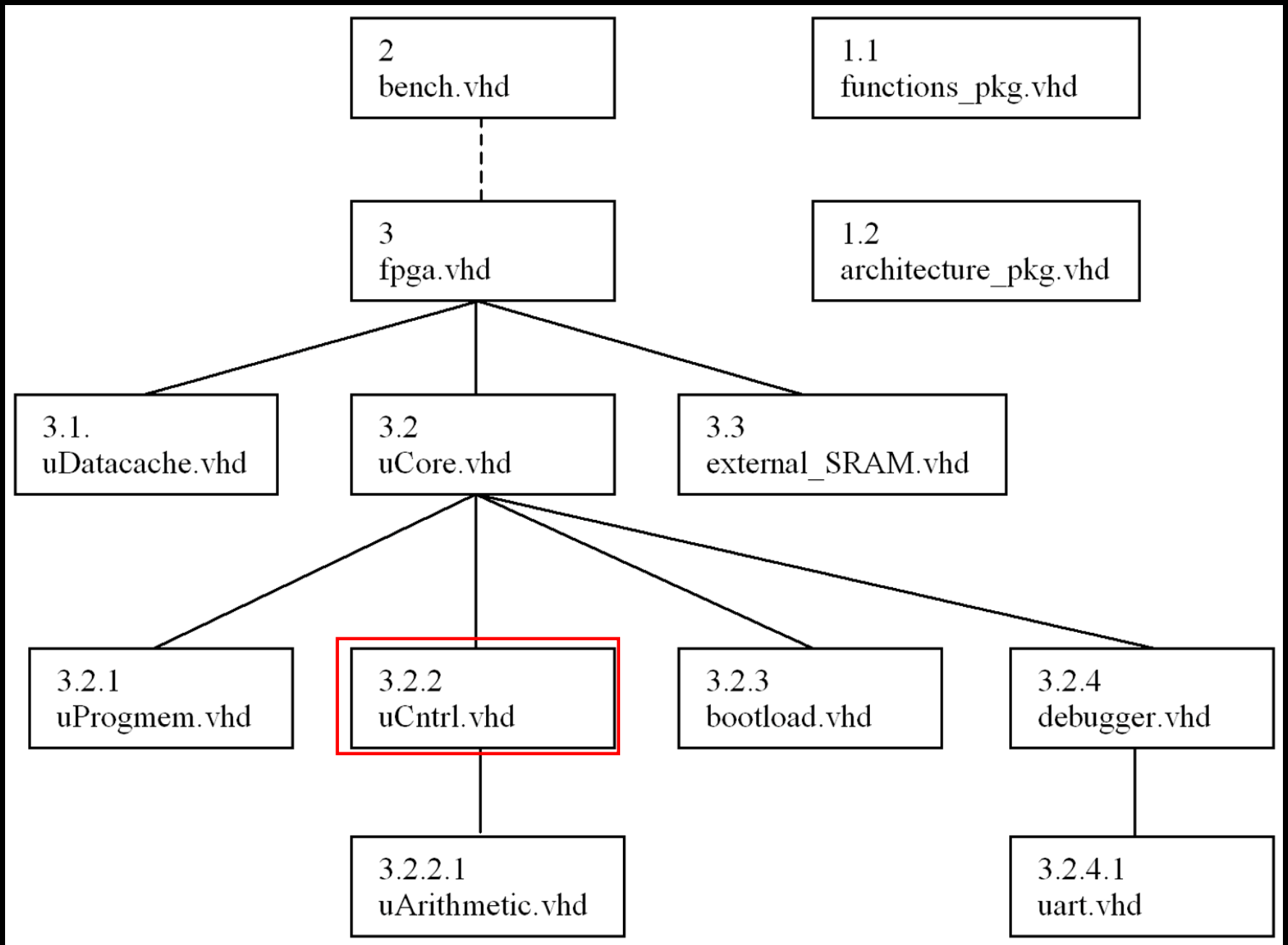
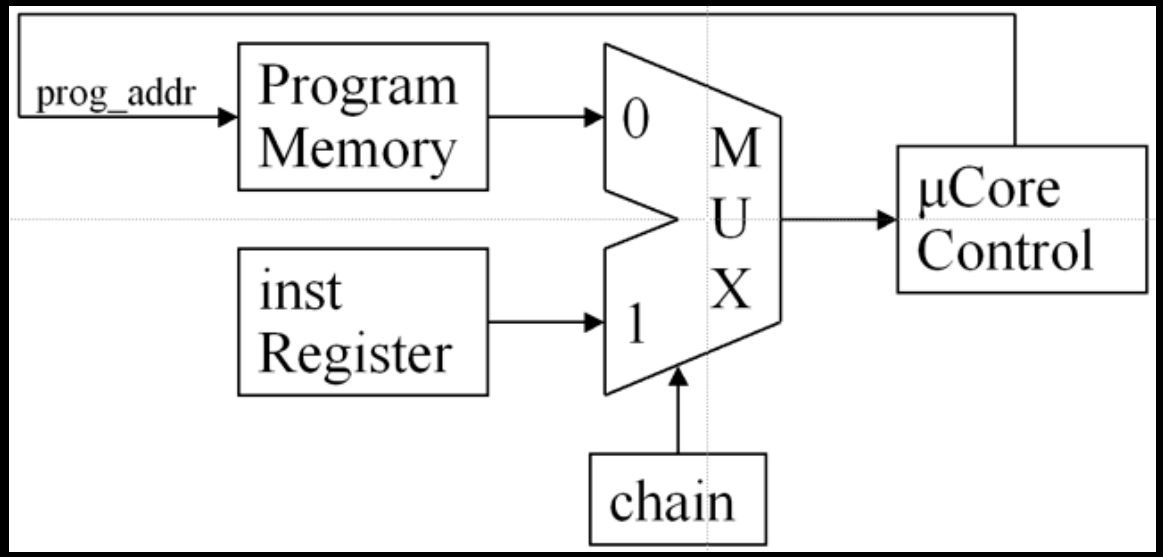
VHDL Structure



2 Cycle Instructions

instruction	2nd cycle
r>	store memory data into TOR
rdrop	store memory data into TOR
exit, iret	store memory data into TOR
?exit	only executed when TOS /= 0: store memory data into TOR
next	only executed when finishing a FOR ... NEXT loop (TOR = 0): store memory data into TOR
@	store memory data into TOS
+!	write (memory data + NOS) back into memory
I	store the sum of TOR and data memory (2nd return stack item) into TOS
IF	in the 1st cycle, the branch address is dropped, in the 2nd cycle the flag as well



Instantiations

- µCore has been ported to Xilinx (XC2S), Lattice (XP2), Altera (EP2), and Actel/Microsemi (A3PE) FPGAs.
- Reference instantiations using an LFXP2-8:

Instruction set	word width	SLICES	data memory	program memory	maximum clock
core	16	988	6k	8k	33 MHz
extended	16	1199	6k	8k	30 MHz
core	27	1259	4k	8k	33 MHz
extended	27	1608	4k	8k	28 MHz
extended and floating point	27	1808	4k	8k	26 MHz
core	32	1432	3k	8k	33 MHz

Links

microCore is available on git:

https://github.com/microCore-VHDL

and here is documentation:

https://github.com/microCore-VHDL/microCore/tree/master/documents