

eSOCFM-1 FPGA System Board

The System-On-Chip Solution

Presented
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April 12, 2003



Summary

- **SOC Development System**
- **FPGA Single Board Computer**
- **Actel ProAsic Plus FPGA Chips**
- **eP32 CPU Core**
- **SRAM, Flash, and EEPROM**
- **Input Output Peripherals**
- **eForth Operating System**
- **Software Development**
- **Demonstrations**

SOC Development System

- **Powerful platform for SOC design and development**
- **SOC system integrates:**
 - CPU
 - Various types of memory
 - Various types of IO devices
 - Real time operating system
 - Application software
- **Board is the ideal solution**

FPGA Single Board Computer

- **Powerful fourth generation FPGA chip as the core**
- **A complete suite of memory chips**
 - 4 MB of flash
 - 256 KB of SRAM
 - 16 KB of serial boot EEPROM
- **An Extensive array of IO devices**
 - Serial and parallel ports
 - SPI, I2C, and LCD interfaces
- **Real time operating system**

FPGA Single Board Computer

- **Minimal instruction set:**
 - Designs scalable from 16 to 64 bits
- **Dual stack architecture:**
 - Return stack for nested return addresses
 - Data stack for nested parameter lists
- **Compute before execution:**
 - All instructions execute in 1 clock cycle
- **Minimized subroutine call and returns:**
 - Support modular and structured programs
 - Seamless integration of high level programming language

Actel ProAsic Plus FPGA Chips

- **0.22u Flash-based FPGA**
- **Secured core for IP distribution**
- **150 K to 1 M system gates**
- **9 KB to 22 KB two-port SRAM**
- **106 IO pins**
- **Up to 350 MHz performance**

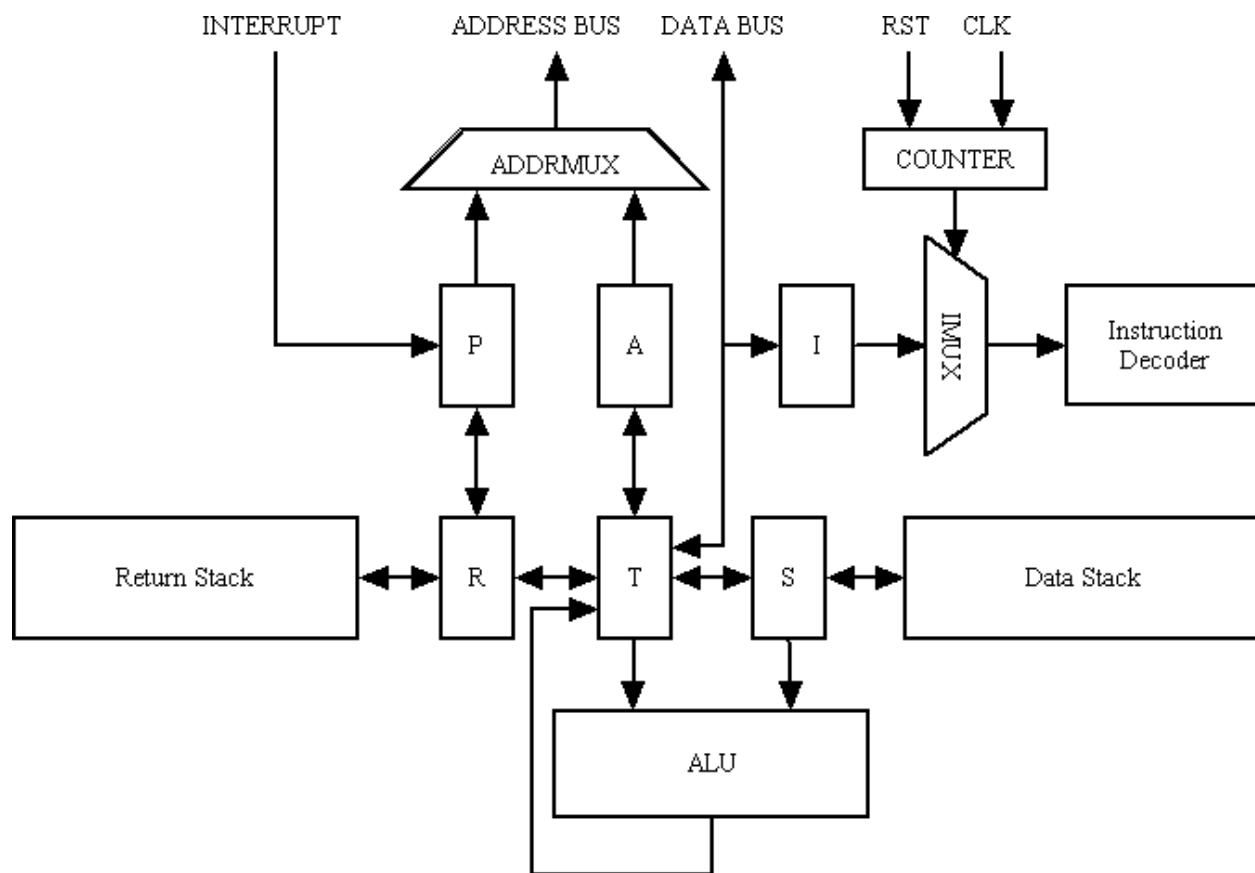
eP32 CPU Core

- **32 bit address and data busses**
- **32 powerful orthogonal instructions**
- **256 level return stack**
- **256 level data stack**
- **Single cycle execution of all instructions**
- **Natural 5 instruction pipeline**

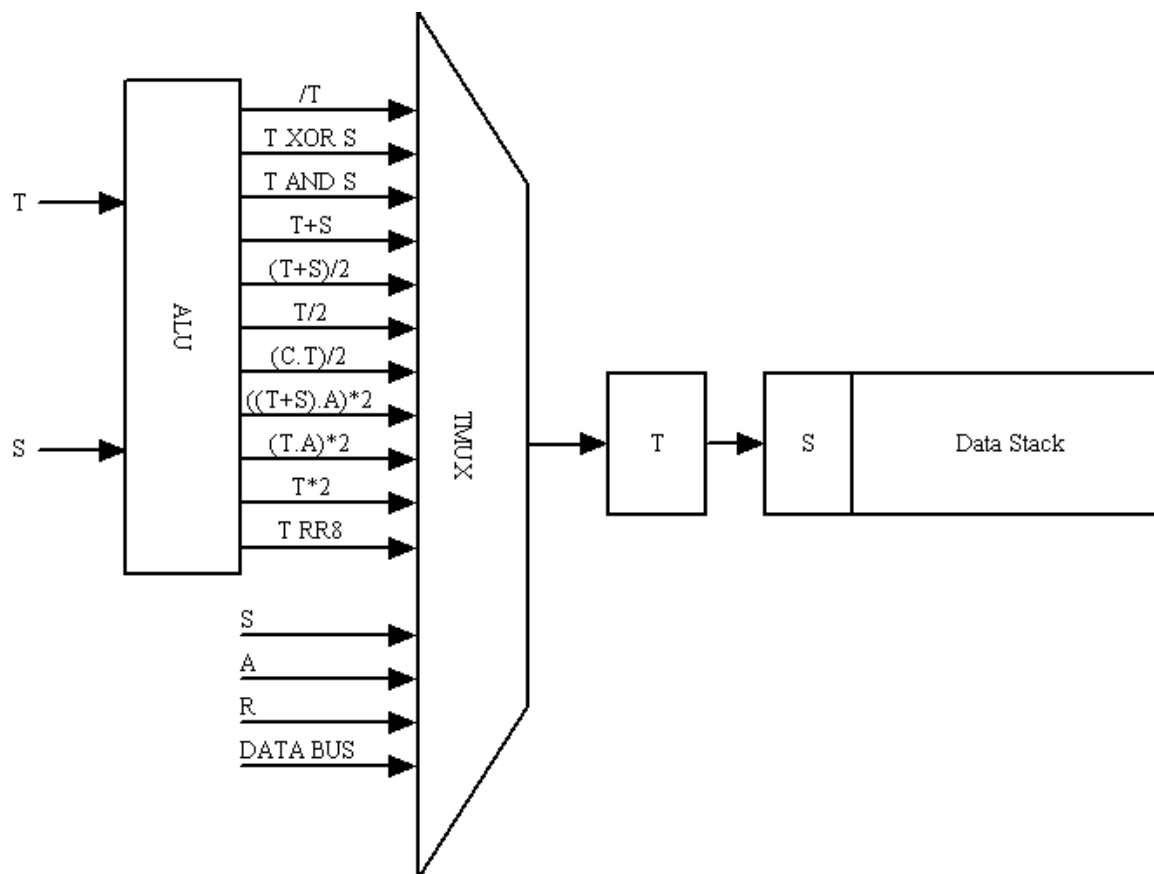
eP32 CPU Core

- **CPU architectural view**
- **ALU and data processing chain**
- **Program and data memory address multiplexer**
- **Return address processing chain**
- **Instruction execution finite state machine**

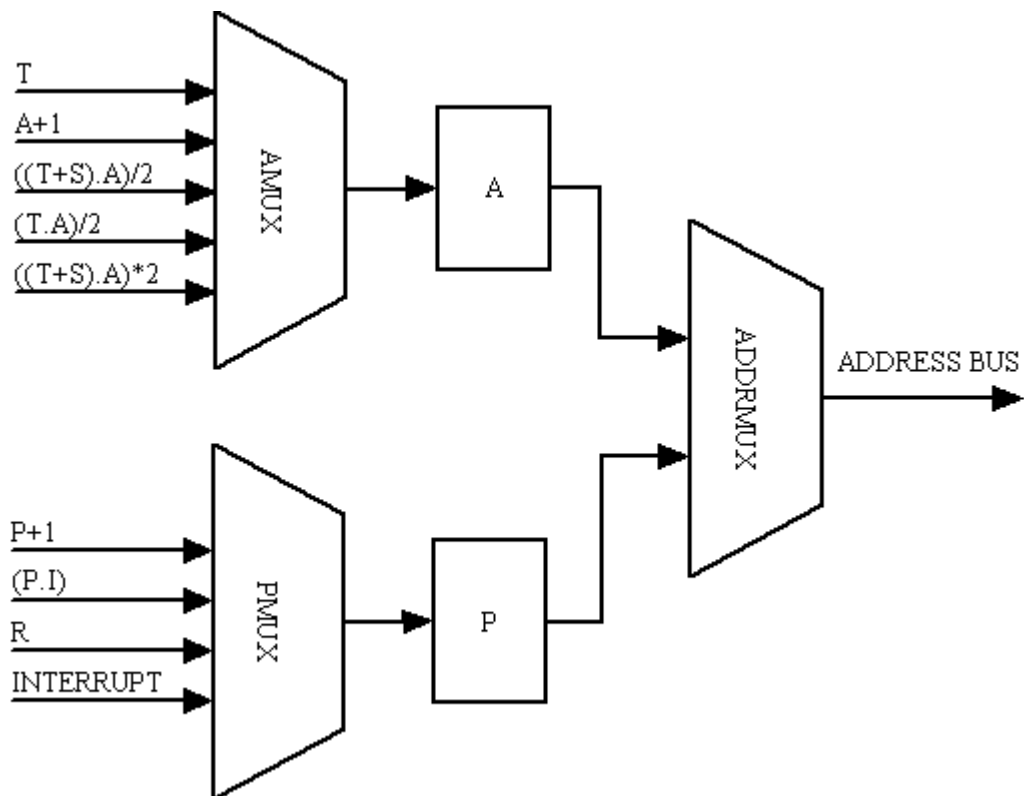
CPU Architectural View



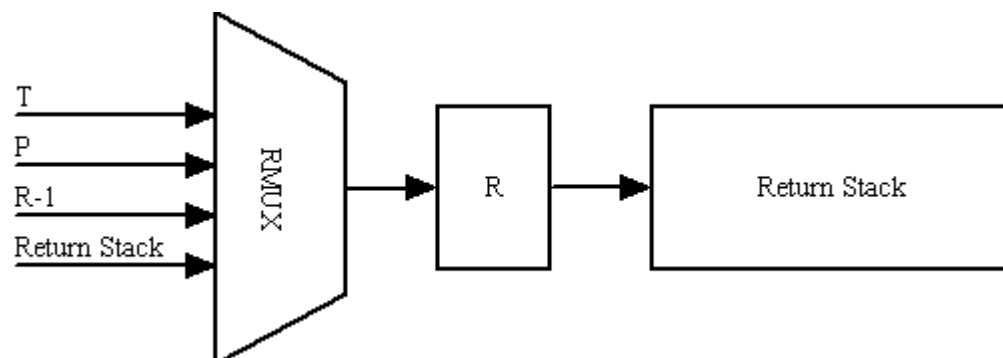
ALU and Data Processing Chain



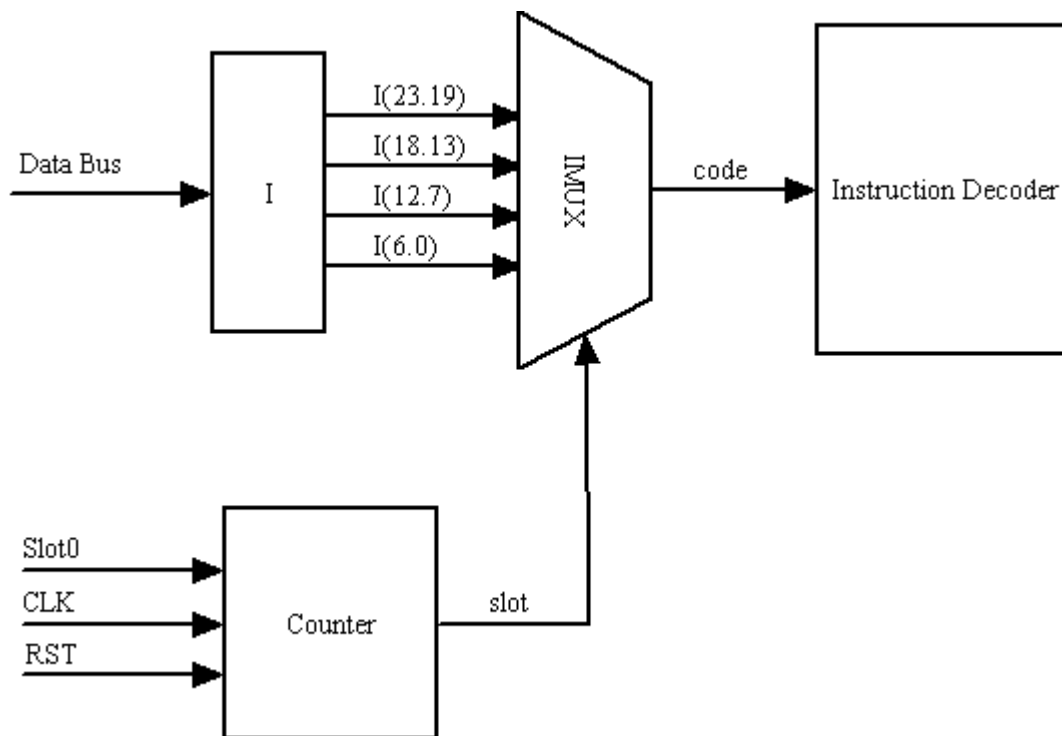
Program and Data Memory Mux



Return Address Processing Chain



Instruction Execution FSM



SRAM, Flash, and EEPROM

- A complete suite of memories
- 4 KB of internal dual port SRAM for stacks and caches
- 256 KB of external SRAM for program and data
- 4 MB of flash memory for mass storage
- 16 KB of serial EEPROM for booting

Input Output Peripherals

- **2 UART ports at 115200 baud**
- **SPI**
- **I2C**
- **16 bit parallel IO port**
- **8 switches**
- **9 LED indicators**
- **LCD interface**

Software Development

- **eForth Real Time Operating System**
- **High level Forth programming language**
- **Interactive software development**
- **Convenient interface to Windows through HyperTerminal**

eForth Operating System

- **Ideal for SOC and embedded systems**
- **Serial port for human interface**
- **Command interpreter**
- **High level command compiler**
- **Low level assembler**
- **Debugging utilities**

eP32 Instruction Set

- **32 orthogonal instructions**
- **Encoded in 6 bit fields**
- **4 Types of instructions:**
 - **6 Program transfer instructions**
 - **5 Memory access instruction**
 - **9 ALU instructions**
 - **8 Register and stack instructions**

Program Transfer Instructions

- **BRA** **Branch always**
- **RET** **Return from subroutine**
- **BZ** **Branch on zero**
- **BC** **Branch on carry**
- **CALL** **Call subroutine**
- **NEXT** **Loop until R is 0**

Memory Access Instructions

- **LD** **Load from memory**
- **LDP** **Load from memory and
increment A register**
- **LDI** **Load immediate value**
- **ST** **Store to memory**
- **STP** **Store to memory and
increment A register**

ALU Instructions

- **ADD** **Add S to T**
- **AND** **AND S to T**
- **XOR** **XOR S to T**
- **COM** **Complement T**
- **SHR** **T shift to right**
- **SHL** **T shift to left**
- **RR8** **T rotate right by 8 bits**
- **MUL** **Multiplication step**
- **DIV** **Division step**

Register and Stack Instructions

- **PUSHS** Duplicate T to S
- **POPS** Pop S to T
- **PUSHR** Push T to R
- **POPR** Pop R to T
- **OVER** Duplicate S over T
- **LDA** Load A to T
- **STA** Store T to A
- **NOP**

Demonstrations

- **Power-up eSOCFM-1 board**
- **Interactive eForth system**
- **Control LED indicators**
- **Operate switches**
- **Download and compile source code**
- **Read and write flash memory**

Concluding Remarks

- **eSOCFM-1 Board is a complete SOC development platform**
- **Ideal for serious and substantial applications**
- **Very useful for FPGA evaluation and experimentation**
- **Integrated operating system allows efficient SOC system design and integration**

Thank you very much!

