Forth Day 2010

Speakers' Schedule

This is the schedule only, other details are at http://www.forth.org/svfig/next.html

========

09:00 Chairman's Welcome --- George Perry

========

09:10 eP32 on Lattice XP2 Brevia Development Kit --- C.H. Ting
Lattice is selling this FPGA kit for $29. Ting is trying to port eP32 to this kit, and will report his progress. The FPGA synthesis, programming and simulation tools are very different from Xilinx's and Altera's so we'll be looking at a work in progress, exploring the challenges of implementing a Forth engine on this platform.

========

09:40 Getting Started with MyForth --- Bob Nash
Bob will give a quick overview of MyForth, along with a quick look at the manual, basic usage and instructions for downloading.

========

09:55 Follow Up to "OO Extensions Considered Harmful" --- Samuel A. Falvo II
The plurality of Object Oriented extensions makes reusing 3rd-party packages unnecessarily complex. Sam will show another coding pattern illustrating how you can write reusable components in plain Forth, with surprising results suggesting it's actually more powerful and even more reusable than what object orientation provides.

========

10:25 Update: Porting Gforth to eCos --- John E. Harbold
John has been able to get Redboot to boot under an i386 KVM virtual environment. Now he's analyzing the Gforth engine to see how to "shoe-horn" it into the eCos source tree.

========

10:35 BREAK

10:50 J1: a Small Forth CPU Core for FPGAs --- James Bowman
James will describe a 16-bit Forth CPU core, intended for FPGAs. The instruction set closely matches the Forth programming language, simplifying cross-compilation. Because it has higher throughput than comparable CPU cores, it can stream uncompressed video over Ethernet using a simple software loop. The entire system (source Verilog, cross compiler, and TCP/IP networking code) is published under the BSD license. The core is less than 200 lines of Verilog, and operates reliably at 80 MHz in a Xilinx Spartan(R)-3E FPGA, delivering approximately 100 ANS Forth MIPS.

========

11:20 Introducing SwiftCore --- Brad Eckert and Leon Wagner
The SwiftCore SC20 is a 32-bit soft CPU designed for SoC applications. Its architecture is equally at home in ASICs and FPGAs, and is compatible with FPGA block RAMs. The instruction set architecture is stack oriented and close to native Forth, so it doesn't need a sophisticated optimizer for high performance. The ISA also supports signed and unsigned 8-bit, 16-bit and 32-bit data types with base+offset addressing modes, frame stacks, and temporary registers. An instantiation of the SC20 on the Lattice XP2 Brevia development kit along with the interactive SwiftX cross compiler will be demonstrated.

========

12:00 Forth Day BBQ --- C.H. Ting
One of our tastiest traditions, lunch in the Peterson Building courtyard, catered by C.H. Ting

========

13:30 Update on GreenArrays --- GreenArrays Staff
Progress and plans of the company; Details of hardware to be delivered in second quarter of 2011; Demonstration of development tools; Discussion of applications. Presented by members of the Technical Staff of GreenArrays, including Chuck Moore, Greg Bailey, Jeff Fox, Charley Shattuck, and others, accompanied by affiliate Michael Montvelishsky who will discuss an application in real time implementation of binocular (stereo) vision."

http://www.greenarraychips.com
Speaker bios: http://www.greenarraychips.com/home/about/bios.html

========

16:00 Fireside Chat --- Chuck Moore

========

17:00 Adjorn

========

17:45 Dinner